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Testing and Reliability Improvement of High Reliability Consumer Electronics Products Manufactured on Printed Circuit Boards

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Abstract:
The design and development of reliable electronic systems is a highly challenging task. In this paper we present the results of research carried out in order to improve the reliability of the printed circuit boards of a high reliability electronic consumer product manufactured locally by the application of accelerated life testing and interconnect stress testing. Reliability improvement is a major goal in many applications. It is especially vital in sensitive devices where human life is involved such as high reliability products, medical electronic systems as well as military applications. Accelerated life testing is a well known technique for reliability improvement of electronic systems. However, its application to printed circuit boards is very difficult. The various types of tests to be performed on the printed circuit board are outlined. A three stage testing procedure to be carried out after visual inspection and microscopic assisted inspection is proposed in order to improve the reliability of the printed circuit boards of the consumer product being manufactured locally. Results of actual implementation of this procedure are presented. This procedure includes microscope assisted visual inspection, interconnect stress testing before part assembly, plus accelerated life testing through thermal and vibration cycling after part assembly. These tests can be used to discover any physical weaknesses in the materials, poor workmanship or design, or the use of any weak parts. They are also used to find the lifetime of the printed circuit boards under accelerated life conditions, and their Weibull probability distribution which can be projected to real operating conditions using Arrhenius equation.[Journal of American Science 2009:5(3) 95-106] (ISSN: 1545-1003)
Key word: Accelerated Life Testing, Interconnect Stress Testing, Printed Circuit Boards, Reliability, Thermal and Vibration Cycling

1. Introduction

The reliability of a system is affected by the reliability of its components and the way they are interconnected to serve its intended mission under certain operating conditions. The reliability of an electronic system is a function of the reliability of its subsystems. It is well known that the reliability of discrete components, digital or analog circuits and their associated interconnects is very low. More important than these is the board on which the components are assembled since its reliability seriously affects the reliability of the overall system. The development of printed circuit boards and the modular design concept in electronic systems has lead to the widespread use of PCBs which are basically boards on which electronic components are assembled. The reliability of the manufactured PCB is a function of both the reliability of the components used on the board and the reliability of the board itself. Many designers forget the importance of the underlying board in the reliability of the overall electronic system.

Printed circuit boards are multi-material structures that are the backbones of the electronics industry. As their performance requirements and complexities increase, the need also increases to better manage factors which affect both performance and reliability including impedance control, warpage, and plated through-hole (PTH) reliability.

A plated-through hole (PTH) in multi-layer printed wiring boards (PWB) is defined as “a hole in which electrical connection is made between internal or external conductive patterns, or both, by plating of metal on the wall of the hole”. Plated through-hole (PTH) assembly continues to be used for a number of applications including military as well as medical electronics. High PTH reliability demands tighter fabrication and assembly controls and tolerances. Laser drilling equipment must be up-to-date and calculations must be accurately performed. Doing so ensures that PTH vias and their annular rings are intact when PCBs undergo multiple heat and reflow cycles. It is very important to consider PTH reliability since PCB real estate, components, vias, and annular ring sizes continue to shrink. One way to improve PTH reliability is in the design stage. This holds true for both the design of the PCB itself and the design of the circuit with a given PCB being used. PCB real estate, along with components, vias, and annular

ring sizes are shrinking. A decade ago, a via hole of 15 to 20 mils with a 5 to 10 mil annular ring was the norm. However, as the board complexity is increasing, via sizes ranging from 7 mils down to 4 mils are more common. As through-hole size (via) shrinks the annular ring size shrinks. This poses major challenges to fabrication and assembly manufacturers in the process. In previous printed circuit boards, two to three mils of play within a 10 mil hole was common. However, nowadays precision laser drilling allows about 0.5 mil or less play since the use of smaller drills has reduced via size to 4 or 5 mils. This means that one mil of play represents 25% of the hole size when a 4 mil via is created. Therefore, tighter fabrication and assembly controls and tolerances, better equipment and well-trained technicians should be used in order to assure high plated through-hole reliability. Sufficient clearance is needed in order to avoid creating break out on internal layers. This condition which may be caused by miscalculations of drill size, pad size, incorrect annular ring size or over-etching at fabrication will result in weak or broken continuity.

The recent trend to increase the packaging density at all levels has resulted in a significant increase in PWB wiring layers and in turn for PTH density in order to communicate between the layers of circuitry. The increase in overall PCB thickness along with the decrease in PTH diameter makes the PTH a main reliability concerns both during the assembly process and subsequent field stresses. The Thermo-mechanical stresses mainly due to mismatch in out-of-plane (z-direction) coefficient of thermal expansion (CTE) between the PTH metal and the laminated material can result in the failure of the PTH which would constitutes an electrical discontinuity caused either by fracture of the plating material at the barrel, fracture at the land-barrel junction, or delamination of the plating from the PWB.

Manufacturers of consumer products are not aware of these issues. They buy their raw printed circuit board from a vendor, and manufacture their consumer goods using them. They expect a good product once they use good parts. However, the reliability problems which are inherent in the printed circuit boards themselves and the challenges in the reliability improvement of their products manufactured using printed circuit boards is to be addressed by researchers. In this paper, we address these issues and present the results of actual implementation of the proposed procedures.

The impact of different types of cured solder mask and mask thicknesses on printed wiring board (PWB) warpage was studied by Ume and Martin (1997). Finite element analysis (FEA) was used to study the sensitivity of board warpage to changes in the mask material properties (different types of solder mask), and to variations in mask thickness. They focused on the sensitivity analysis of the influence of cured solder mask and variations in mask thickness on PWB warpage and carried out their study with four different board designs, and developed guidelines which should be observed when selecting masking materials.

The reliability performance of the PTHs when subjected to T/C (Temperature Cycle) stresses was discussed by Goval et al. (1997). During the initial reliability stressing through 1000 T/C `B' (-55 to 125°C) and T/C `C' (-65 to 150°C) electrical opens were observed. Physical analysis showed that the opens were due to barrel cracking of the PTHs. Extensive mechanical modeling and experimental validation were used to suggest changes in the materials, process and design to eliminate barrel cracking in high aspect ratio PTHs.

Simulation and experimental verification procedures for investigating thermally induced warpage of printed wiring boards (PWB) and printed wiring assemblies (PWAs) were presented by Zwemer et al. (2004) due to its importance in managing the manufacturing yield and reliability of electronic devices.

The reliability of plated through holes (PTH's) as "PTH life curves" which plot cycle to fail vs. temperature for the entire range of field, accelerated thermal cycling, and assembly reflow thermal exposures on a printed wire board (PWB) or laminate chip carrier (LCC) were presented by Knadle and Jadhav, (2005). The curves represent years of testing with the current induced thermal cycle test (CITC) covering different resin systems, via constructions, and metal finishes. The curves reveal a number of critical factors in PTH reliability including the significant effect of lead (Pb) free reflows, resin system formulation, and copper plate chemistry on via life. They developed a finite element model for one of the PTH constructions and provided examples of cumulative damage life projections for a number of PWB and LCC cases using the life curves.

The reliability of electronic systems can be improved using derating and accelerated life testing. Moreover, the integration of various subsystems by a more modern and reliable components can improve the reliability of electronic systems as shown by Peiravi, 2008. Moreover, the reliability of electronic systems can be improved using derating and accelerated life testing as shown by Peiravi, 2009. The stress in

this research is placed on improving the reliability of the printed circuit boards in a high reliability consumer electronic product which are highly critical in the overall reliability of consumer electronic systems.

Tests on Printed Circuit Boards

There are various types of tests which must be performed on the printed circuit board before and after parts are assembled on them. Some of these tests are destructive in nature, while others are not. The destructive tests are usually designed to discover the upper or lower bounds of a physical parameter such as glassification temperature T_g, decomposition temperature T_d, or lifetime under accelerated conditions while the non-destructive tests are usually designed for qualification and screening purposes.

Printed circuit boards should undergo the tests listed in Table 1 based on the type.. of application

Table 1. The Various Test Types for Printed Circuit Boards

Test	Test Type	Performed for IPC Class 3	Performed for High Reliability	Performed for Military
1	Visual and	X	X	X
2	Etchback		X	
3	Plating adhesion	X	X	X
4	Microsectioning		X	X
5	Terminal pull	X	X	X
6	Copper strike		X	
7	Warp and twist	X	X	X
8	Traceability		X	
9	Water absorption		X	
10	Copper		X	
11	Solderability	X	X	
12	Pth structure		X	X
13	Fungus resistance		X	
14	Mechanical shock		X	
15	Vibration		X	
16	Thermal shock		X	X
17	Thermal stress		X	X
18	Outgassing		X	
19	Interconnection	X	X	X
20	Insulation resistance	X	X	X
21	Dielectric strength	X	X	X
22	Hot oil resistance	X		X
23	Moisture resistance	X	X	X
24	Current carrying	X	X	
25	Internal shorts	X	X	
26	Circuitry electrical		X	X
27	Flammmability	X	X	X

for which they are intended before the assembly of electronics components. The testing requirements for high reliability products are almost as stringent as that of military applications, or even more stringent as you can see from the Table. The only point is that consumer products can be tested for the less stringent industrial temperature range of -15 ℃ to +85 ℃ or even commercial temperature range of 0 ℃ to 70 ℃ , while military products must be able to withstand temperature stresses well beyond the military range of -55 ℃ to +125 ℃ .

The reliability of printed circuit boards may be improved if proper procedure is established in accordance with the following test standards for electrical, thermal, mechanical, and physical properties of PCBs according to Tables 2, 3, 4 and 5 in addition to tape tests, visual and microscope assisted visual inspection meant to reveal gross physical problems with the board.

Microscopic Assisted Visual Inspection

One of the earliest tests to be performed on the bare printed circuit boards before components are assembled onto them is visual inspection. This can be assisted with a microscope to gain more information. Some physical flaws due to the initial board preparation actions such as drilling may be seen such as shown in Figure 1.

Accelerated Life Testing of Printed Circuit Boards

Moreover, accelerated life testing of the board may be used after all these tests are performed in order to measure its maximum tolerance and to quantify the lifetime of the board under accelerated conditions which may be projected to real life operating conditions using Arrhenius equation.

The accelerated life testing should be done in three phases:

Table 2. Standard Electrical Tests for Printed Circuit Boards

Test No.	Quantity Being Tested	Units	Test Method
1	Dielectric Constant @ 1MHz		IPC TM-650 2.5.5.3
2	Dielectric Constant @ 1GHz		IPC TM-650 2.5.5.9
3	Dissipation Factor@ 1MHz		IPC TM-650 2.5.5.3
4	Dissipation Factor@ 1GHz		IPC TM-650 2.5.5.9
5	Volume Resistivity	MΩ-cm	IPC TM-650 2.5.17.1
6	Surface Resistivity	MΩ	IPC TM-650 2.5.17.1
7	Electrical Strength	Volts/mil (kV/mm)	IPC TM-650 2.5.6.2
8	Dielectric Breakdown	kV	IPC TM-650 2.5.6
9	Arc Resistance	Sec	IPC TM-650 2.5.1

Table 3. Standard Thermal Tests for Printed Circuit Boards

Test No.	Quantity Being Tested	Units	Test Method
1	Glass Transition Temperature (Tg) TMA	°C	IPC TM-650 2.4.24
2	Glass Transition Temperature (Tg) DSC	°C	IPC TM-650 2.4.25
3	Decomposition Temperature (Td) Initial	°C	IPC TM-650 2.4.24.6
4	Decomposition Temperature (Td) 5%	°C	IPC TM-650 2.4.24.6
5	T260	Min	IPC TM-650 2.4.24.1
6	T288	Min	IPC TM-650 2.4.24.1
7	T300	Min	IPC TM-650 2.4.24.1
8	CTE (x,y)	ppm/°C	IPC TM-650 2.4.41
9	CTE (z) < Tg > Tg	ppm/°C	IPC TM-650 2.4.24
10	z-axis Expansion (50-260ºC)	%	IPC TM-650 2.4.24

Table 4. Standard Mechanical Tests for Printed Circuit Boards

Test No.	Quantity Being Tested	Units	Test Method
1	Peel Strength to Copper (1 oz/35 micron) After Thermal Stress At Elevated Temperatures After Process Solutions	lb/in (N/mm)	IPC TM-650 2.4.8
2	Young's Modulus	Mpsi (GPa)	IPC TM-650 2.4.18.3
3	Flexural Strength	kpsi (MPa)	IPC TM-650 2.4.4
4	Tensile Strength	kpsi (MPa)	IPC TM-650 2.4.18.3
5	Compressive Modulus	kpsi (MPa)	ASTM D-695
6	Poisson's Ratio (x, y)		ASTM D-3039

Table 5. Standard Physical Tests for Printed Circuit Boards

Test No.	Quantity Being Tested	Units	Test Method
1	Water Absorption	%	IPC TM-650 2.6.2.1
2	Specific Gravity	g/cm^3	ASTM D792 Method A
3	Thermal Conductivity	W/mK	ASTM E1461
4	Flammability	Class	UL-94

1-Perform interconnection stress testing before parts are assembled onto the board.
2-Perform thermal stress cycles after parts are assembled onto the board
3-Perform vibration stress testing after the boards pass the first two parts of the testing procedure.

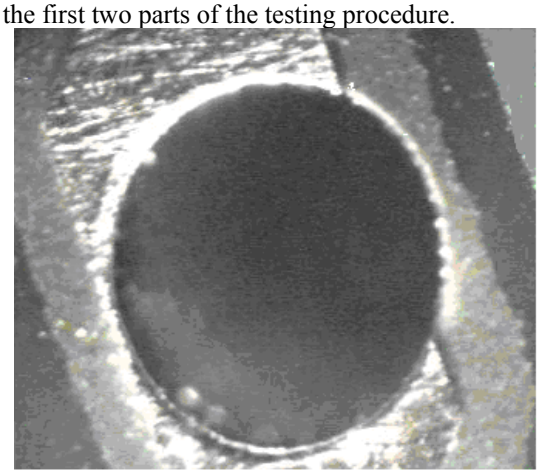

Figure 1. An Image of a Plated Through Hole on a Printed Circuit Board Showing Damage to the Conductor around the Hole

Destructive Accelerated Life Testing to Determine the PCB Glassification Temperature

The glassification temperature of the printed circuit boards being used must be tested in order to make sure that no weak PCBs are being used which may be bought through unreliable vendors. For this reason, an accelerated thermal cycling test must be used which takes the board's surface temperature from room temperature to beyond its glassification temperature and back. This test was carried out on a sample FR4 laminate. The board was exposed to repeated cycles of thermal stress which took the board to a temperature above its expected glassification temperature as shown in Figure 2.

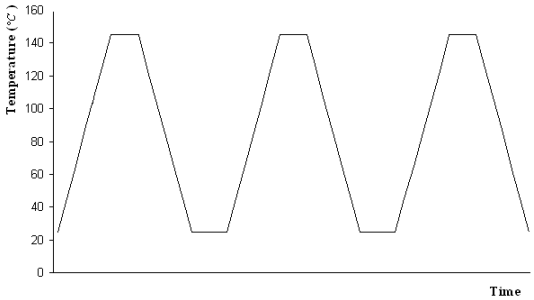

Figure 2. Thermal Stress Cycling to Test for the Board's Glassification Temperature

The board started to burn and there was severe damage to the mental interconnect and the woven fiber on the surface of the PCB as shown in Figure 3 and Figures 4. The sample used for this study was as FR4 with a glassification temperature of 140 ℃ .

Interconnect Stress Testing

Before the components are assembled on the printed circuit board, it should be tested for PTH reliability. Mechanical or thermal stress cycling using external sources of stress were used in the past. However, these techniques are expensive to implement and time consuming. A more recently developed technique that is used in this research is interconnect stress testing.

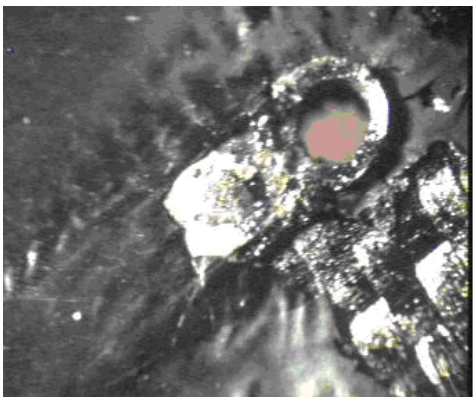

Figure 3. Physical Damage Done to the Board's Surface Uncovering the Underlying Woven Structure of the PCB After the Test

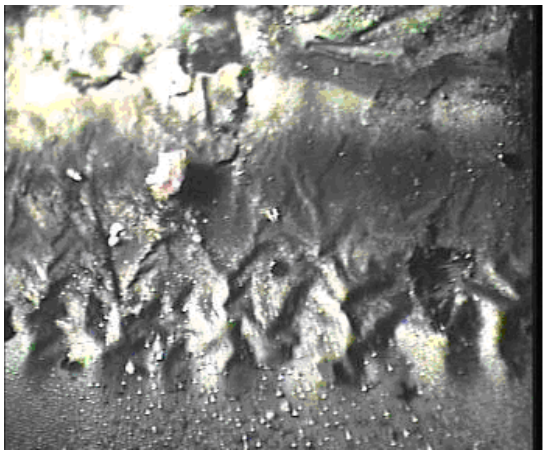

Figure 4. Physical Damage Done to the Board's Metal Interconnect After the Test

The technique is based on the design of two similar patterns on a piece of a printed board which consist of a continuous interconnection of PTHs on a sample coupon as shown in Figure 5. This coupon is usually manufactured as an attachment to the printed circuit board of the electronic circuit being manufactured.

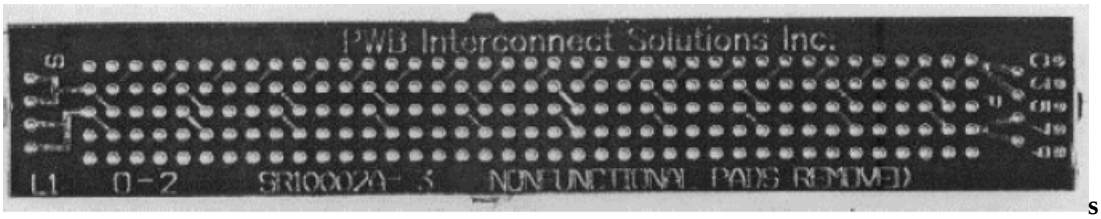

Figure 5. A Typical IST Test Coupon (from PWB Interconnect Solutions, Inc)

During the test, a direct current is applied to one and not applied to the other, and the resistance of the total interconnect path is monitored while the thermal stress cycling is applied. The resistance should be somewhere between $150m\Omega$ and 1.5Ω. The temperature cycle to be applied is supposed to vary from $25℃$ to $+150℃$ and then back to room temperature again. The current should be applied for about three minutes and then removed and the sample should be allowed to cool down back to room temperature. Should the cooling be not fast enough, a forced cooling method should be applied. As the test progresses, the stresses on the interconnections cause rapid wear on the metal layers and the plated through holes. Any weaknesses in the path of the flow of current would lead to deterioration as a result of which the resistance of the circuit would increase as shown in Figure 6. Total destruction of the path of the flow of current would result in an open circuit which marks the end of the destructive testing procedure Of course, even a given percentage increase in the resistance can be used as an indication of occurrence of fatigue and could be used to stop the testing. This is an IPC approved (TM-650 2.6.26) test method [7].

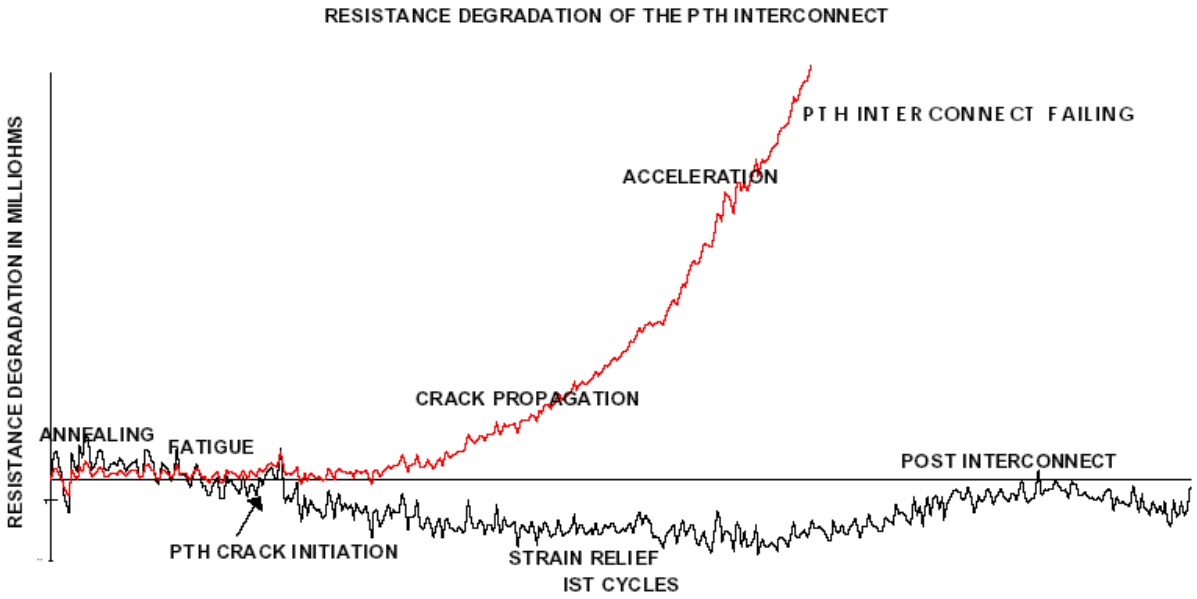

Figure 6. Resistance Degradation of the PTH Interconnect During an Accelerated Interconnect Stress Testing adopted from IPC-TM-650 [7]

The resistance of the path is given by

$$R_t = R_m(1 + \alpha_T[T_h - T_m])$$

where R_m is the resistance at room temperature, α_T is the coefficient of thermal resistance of the PTH interconnects and T_h is the high temperature, and T_m is the room temperature. Therefore, the resistance can be measured and plotted as IST thermal stress cycles are applied.

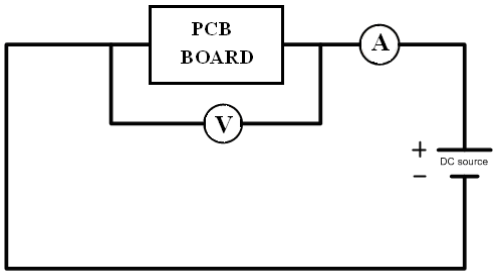

Figure 7.The Circuit used for IST Thermal Stress Cycling

The application of the IST thermal stress can be implemented by applying a DC voltage source to the test subject and measuring the current as shown in Figure7.

These tests were performed on the test coupons built along the edges of ten samples on the electronic circuits of the consumer product. The results of this interconnect stress testing are tabulated in Table 6.

Since each IST test cycle is designed to take only about 10 minutes, the lifetime of each sample being subjected to a destructive IST test is measured and..tabulated in. Table 6. This data is then used to compute the Weibull probability distribution function for the accelerated lifetime of the samples tested as shown in Figure 8. The slope of the line and the t-axis crossing of the plot can be used to find the two parameters of the Weibull probability distribution function.

Table 6. Accelerated Lifetime of Ten Samples of a Printed Circuit Board Subjected to IST Testing

Board being tested	No. of cycles IST was applied	Results	Measured lifetime of the board under test (min)
1	350	An open circuit resulted at the end of the test	3500
2	425	An open circuit resulted at the end of the test	4200
3	150	An open circuit resulted at the end of the test	1500
4	152	An open circuit resulted at the end of the test	1520
5	240	An open circuit resulted at the end of the test	2400
6	190	An open circuit resulted at the end of the test	1900
7	280	An open circuit resulted at the end of the test	2800
8	220	An open circuit resulted at the end of the test	2200
9	330	An open circuit resulted at the end of the test	3300
10	270	An open circuit resulted at the end of the test	2700

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Performing Thermal Stress Cycles after Parts are Assembled on the Board

Once the operations of phase 1 of the reliability improvement program were implemented, the second phase of testing was carried out. This phase is a non-destructive highly accelerated life test which was designed for the industrial range of temperatures from $-15°C$ to $+85°C$ as shown in Figure 9 below with each thermal stress cycle designed to take only 18 minutes with 5 minute stops at the high and low ends.

In this research, the functional circuit tests were designed so that functional tests were continuously carried out during the stress testing. Therefore, the actual tests were run much faster averaging 11 minutes for each cycle as shown in Figure 10. Of course, the tests do not follow the ideal form shown in Figure 9 exactly since the unit under test does not exactly follow the chamber temperature.

This is so due to many factors such as the geometry of the chamber, the size and physical characteristics of the printed circuit board being tested and the thermal characteristics of the heating .and .cooling. systems .of .the .chamber.

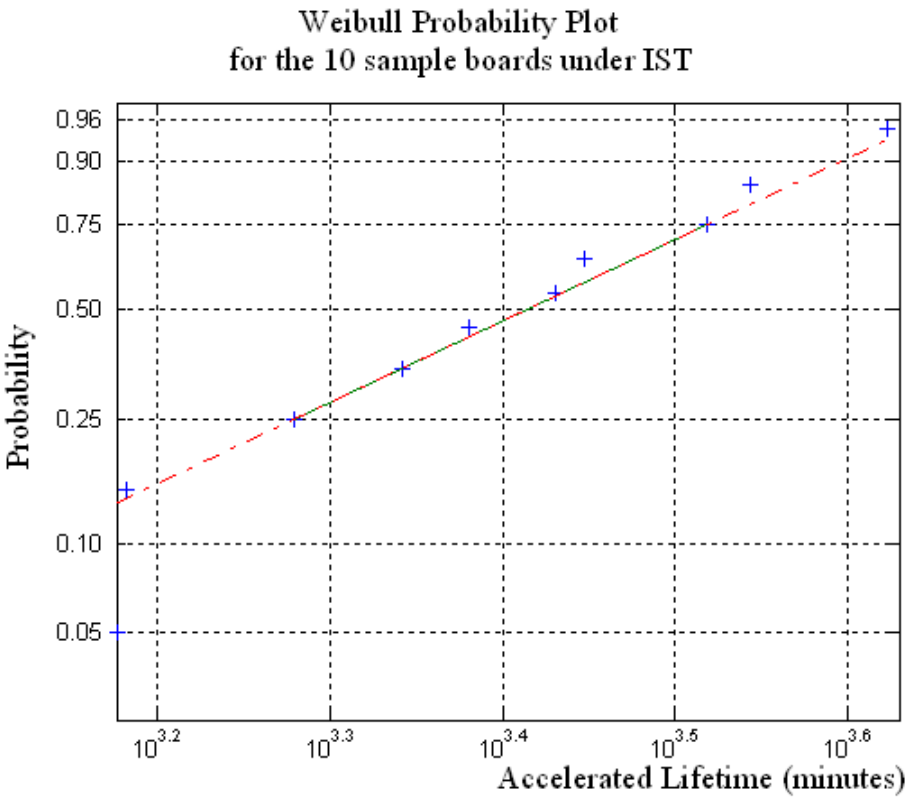

Figure 8. The Weibull Probability Plot for the Accelerated Lifetime of the Samples Tested

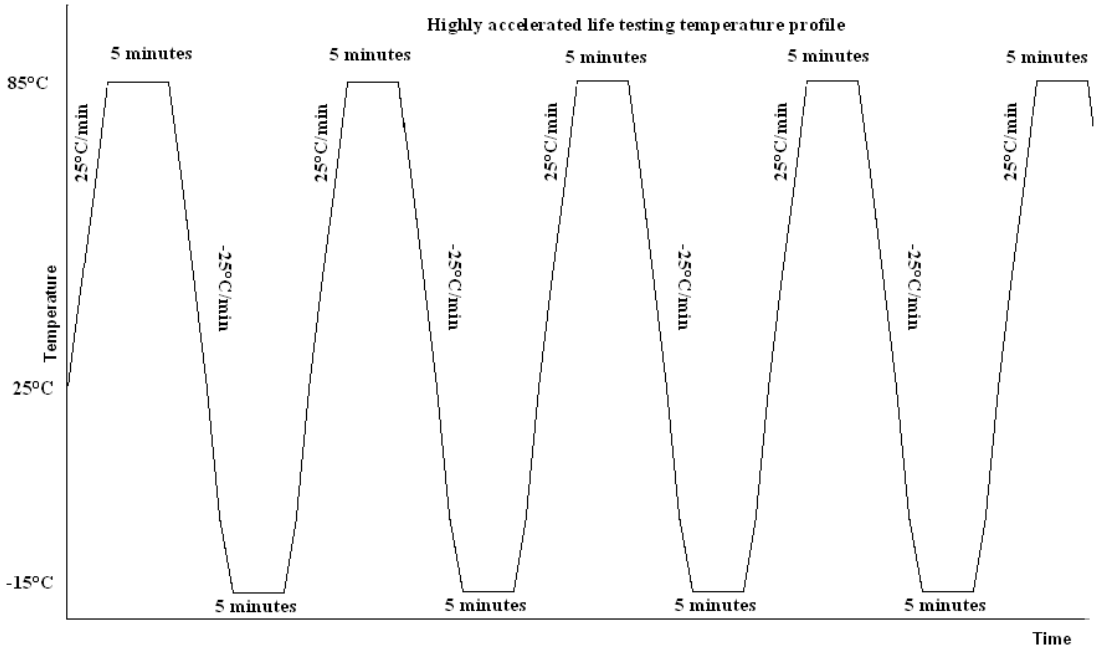

Figure 9. The Temperature vs. Time Profile for the Highly Accelerated Life Testing of the Printed Circuit Board After Part Assembly

For example, we show a sample of the measurements of temperature of one of the printed circuit boards being tested with that of the chamber in Figure 10.

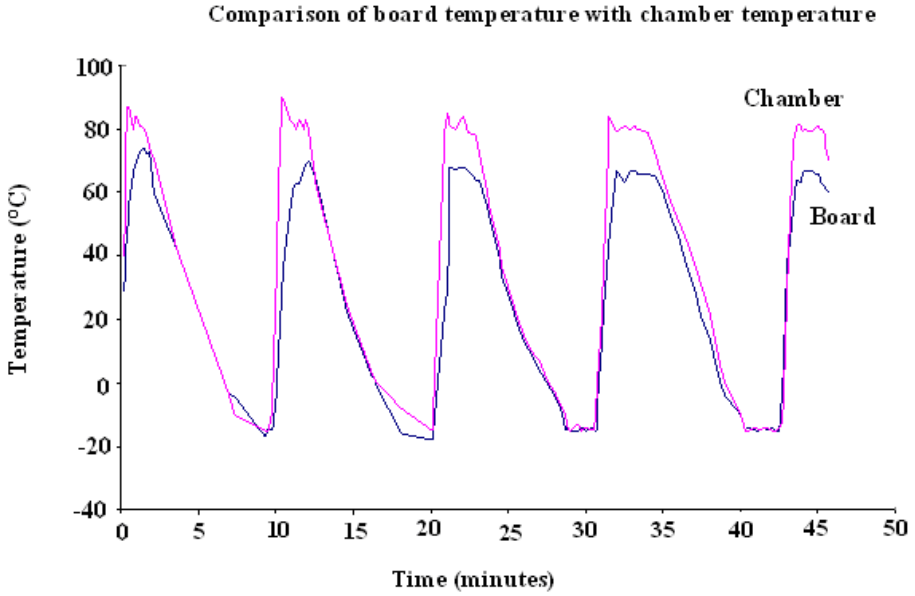

Figure 10. The Temperature Profile for the Board as Compared with the Chamber Showing a Lag in the Board Following the Temperature of the Chamber

Performing Vibration Stress Cycles after Parts are Assembled on the Board

Another form of stress on printed circuit boards is vibration. This could be applied in delivery, or in an actual application of the board in its intended operating conditions. Some potential forms of damage due to excessive vibrations are sketched in Figure 11 as reported in the literature.

The boards being tested should be attached to a special fixture and assembled onto a vibration induction system with accelerometers attached to them in order to measure their response to the vibration.

A six degree of freedom system should be used for the measurements. This information should be used to adjust the fixture in such a used to adjust the fixture in such a manner as to apply the vibration uniformly over all parts of the board being tested. The vibration stress should be started at 3-5GRMS and stepped up in 3 GRMS steps until the product under test fails. Once corrective action is implemented on the units, the testing must only go up to as high as the design specifications state per the operating conditions of the device under test. The board should be held at each vibration level for 10 minutes.

Once the above three steps were implemented and the expected reliability level for the product was achieved, the boards were qualified in a mixed thermal-vibration environment with a temperature variation from $-15°C$ to $+85°C$ plus a vibration test performed on the high and low temperatures as shown in Figure 12.

Results

In this paper the results of the development of a testing procedure for high reliability consumer electronics printed circuit boards is presented. The. tests. were. conducted .and .the .flaws in .the

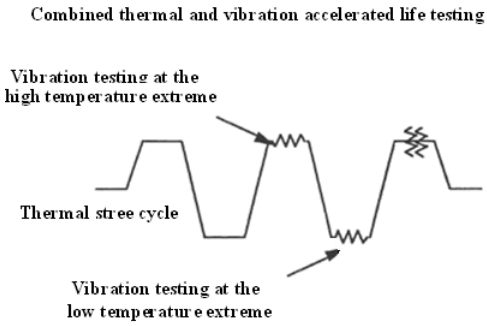

Figure 12. The Combined Temperature and Vibration Accelerated Life Test

PCB and the various failure mechanisms such as delamination and PTH failure were detected. The design corrections were put into effect and the accelerated life tests on ten samples of printed circuit board were performed to determine its Weibull probability distribution. The accelerated life cycle stress testing procedures for thermal

cycling, vibration cycling and mixed cycling were developed and implemented at the factory. Results have shown that the product was able to acquire a high reliability status amongst the electronic consumer products being manufactured locally. There were many problems and challenges which were faced during the implementation phase of this project. Some were overcome with engineering redesign and hard work, while others require more investment by the local manufacturer.

Acknowledgement

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