Controlling of Analog Capture Circuit and Digital Analog Converter for Spartan-3E FPGA Starter Kit

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Abstract: The analog capture circuit and Digital Analog Converter Controller (DAC) is very useful to apply and test the digital algorithms which are executed inside the Spartan-3E FPGA. A VHSIC Hardware Description Language (VHDL) code for controlling of Analog Capture Circuit and DAC of Spatan-3E FPGA Starter Kit board has been designed, implemented and tested. The code is based on finite state machine for each component. The VHDL code and its results are presented.

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1. Introduction

Nuclear measurements for nuclear safeguards applications using nuclear spectrometers with analog shaping are being replaced by digital systems that can provide higher throughput, better energy resolution and better stability. In the past, most spectroscopic systems used analog shaping, mostly Gaussian, to process detector signals. The peak of the shaped signal was digitized with an ADC and sorted into an energy spectrum using MCA. However, in the last years, systems with Digital Signal Processing (DSP) have started to replace the conventional analog systems to improve the performance and to build small handhold solutions [1]. The DSP algorithms could be executed inside a Field Programmable Gate Array (FPGA). The Analog to Digital Converters (ADCs), and their counterparts, Digital to Analog converters (DACs) are electronic components that mostly used in digital systems because digital signals cannot be used directly, as all the real world signals are more or less analog in nature; so that the analog signal first gets converted into digital one, then the processing is done on the digital signal, and finally the processed output is again converted into analog signal so that it can be used with other systems [2]. The analog capture circuit and DAC controller is very useful to apply and test the DSP algorithms which are executed inside the Spartan-3E FPGA. The Spartan-3E FPGA Starter Kit board includes two-channel analog capture circuits and an SPI-compatible, four-channel, serial 12-bit DAC. Each analog capture circuit channel consist a programmable scaling amplifier and 14-bit ADC. The amplifier, ADC and DAC are serially programmed or controlled by the FPGA [3]. Figure 1 shows the schematic diagram of amplifier, ADC and DAC [4]. The maximum range of the ADC is ±1.25 V which is centred on 1.65 V (reference voltage). The gain of each amplifier is programmable according the input voltage range [3]. Table (1) lists the interface signals between the FPGA and the amplifier, ADC and DAC. Istiyanto, J.E carried out and tested a VHDL design of a controller for the amplifier and ADC present on a Spartan-3E Starter Kit board [5]. D. Sillage developed Verilog modules for ADC, programmable scaling amplifier and DAC controlling [6].

2. Design and Implementation

The code is designed to control the amplifier, ADC and DAC on board the Spartan 3E FPGA. FPGA is programmed using VHDL. The VHDL code design based on Finite State Machine (FSM) is used to control the amplifier, ADC and DAC of Spartan 3E FPGA starter kit. FSM constitute a special modeling technique for sequential logic circuits. Such a model can be very helpful in the design of certain types of systems, particularly those whose tasks form a well-defined sequence [7]. State machines can usually be modelled using a case statement in a process. The state information is stored in a signal. The multiple branches of the case statement contain the behaviour for each state [8].

The amplifier, ADC and DAC are connected together through Spartan 3E FPGA using the signals in Table 1. The aim of this work is achieved through using these signals to control them and to pass the outputs through them. Figure 2 shows the block diagram of three components and their signal with Spartan 3E FPGA.

The initial state machine S0 is set pins and are shown in Figures 3, 4, 5 respectively.

timing signals for amplifier, ADC and DAC before the system is running in earnest. The state diagrams of FSMs for controlling the amplifier, ADC, DAC.

The design is then synthesised ("compiled"), placed, and routed on the FPGA using the ISE 9.2i software. The configured FPGA is tested and verified using an Electronic Explorer as shown in figure 6.

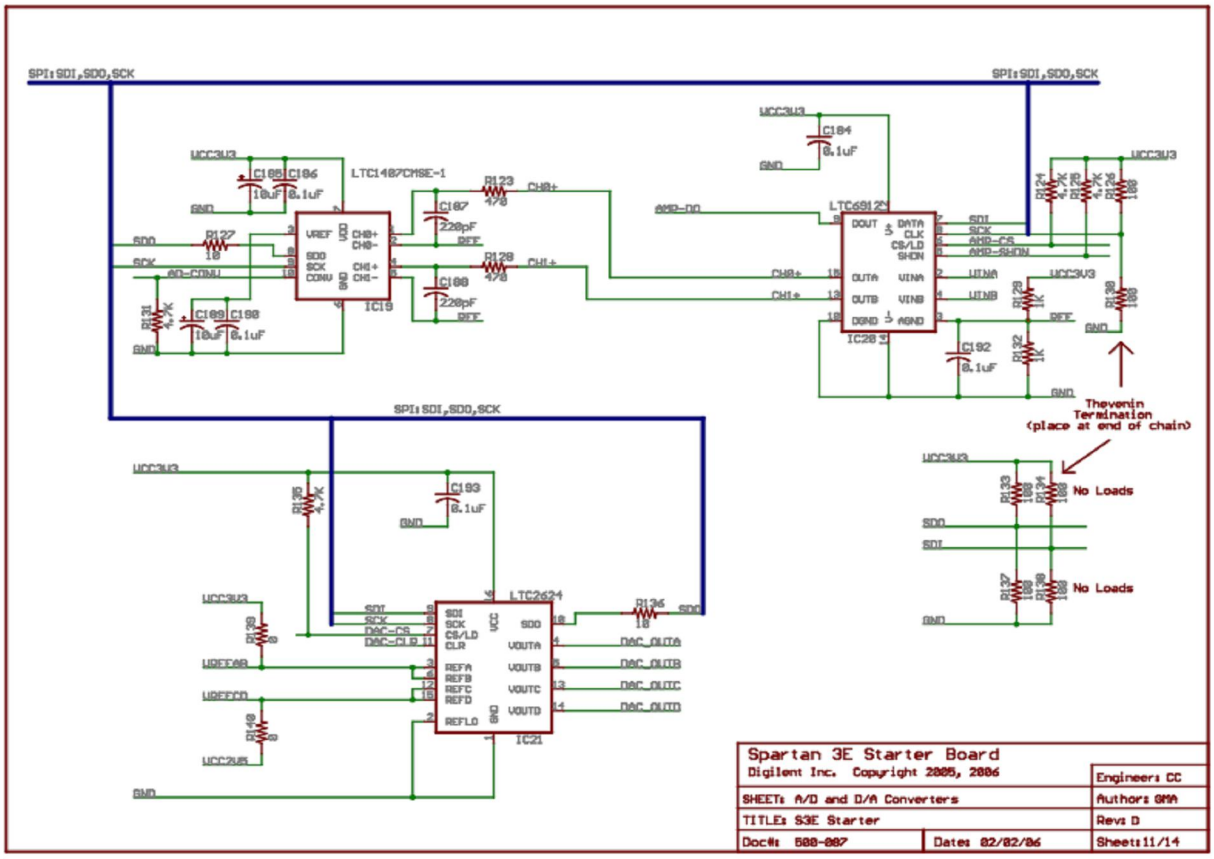

Figure 1. the schematic diagram of amplifier, ADC and DAC

Table 1. AMP, ADC and DAC INTERFACE SIGNAL [3]

Signal	FPGA Pin	Direction	Description
SPI_MOSI	T4	FPGA→AD FPGA→DAC	Serial data: Master Output, Slave Input.
AMP_CS	N7	FPGA→AMP	Active-Low chip-select. The amplifier gain is set when signal returns High
SPI_SCK	U16	FPGA→AMP FPGA→ADC FPGA→DAC	Clock
AMP_SHDN	P7	FPGA→AMP	Active-High shutdown, reset
AD_CONV	P11	FPGA→ADC	Active-High shutdown and reset.
SPI_MISO	N10	FPGA←ADC	Serial data: Master Input, Serial Output. Presents the digital representation of the sample analog values as two 14-bit two's complement binary values.
		FPGA←DAC	Serial data: Master Input, Slave Output
DAC_CS	N8	FPGA→DAC	Active-Low chip-select. Digital-to-analog conversion starts when signal returns High.
DAC_CLR	P8	FPGA→DAC	Asynchronous, active-Low reset input

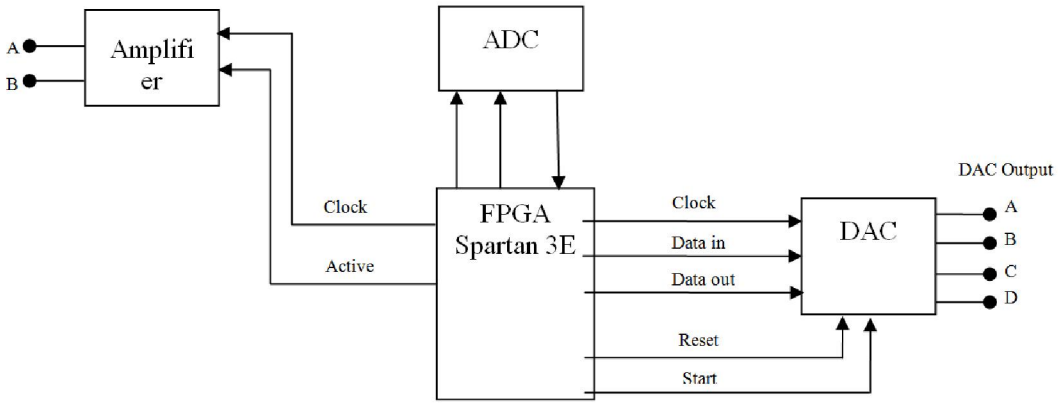

Figure 2. Block diagram of amplifier, ADC, DAC and its signals

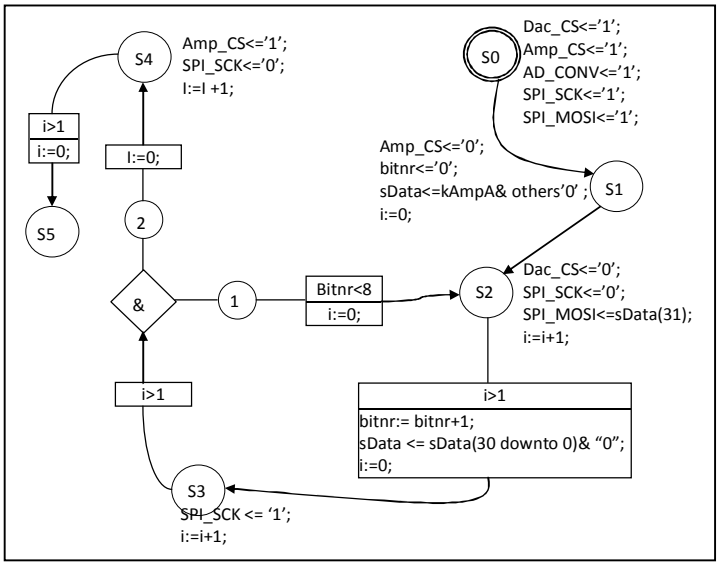

Figure 3.State diagram of FSM for controlling the amplifier on board Spatan 3E FPGA Starter kit

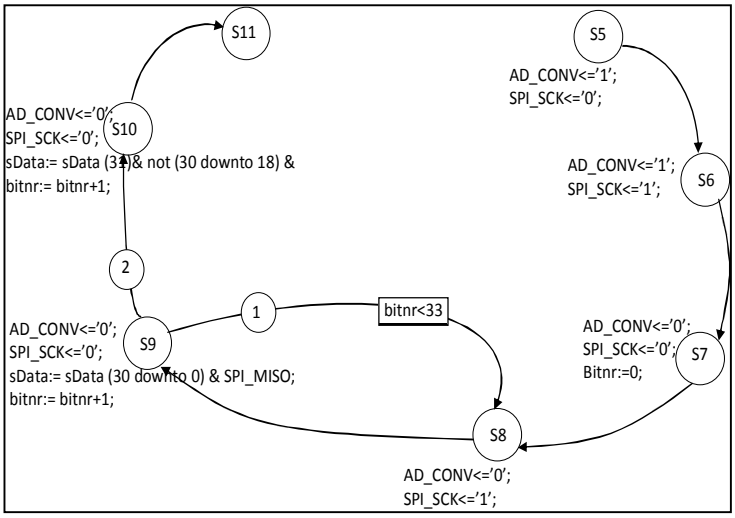

Figure 4. State diagram of FSM for controlling the ADC on board Spatan 3E FPGA Starter kit

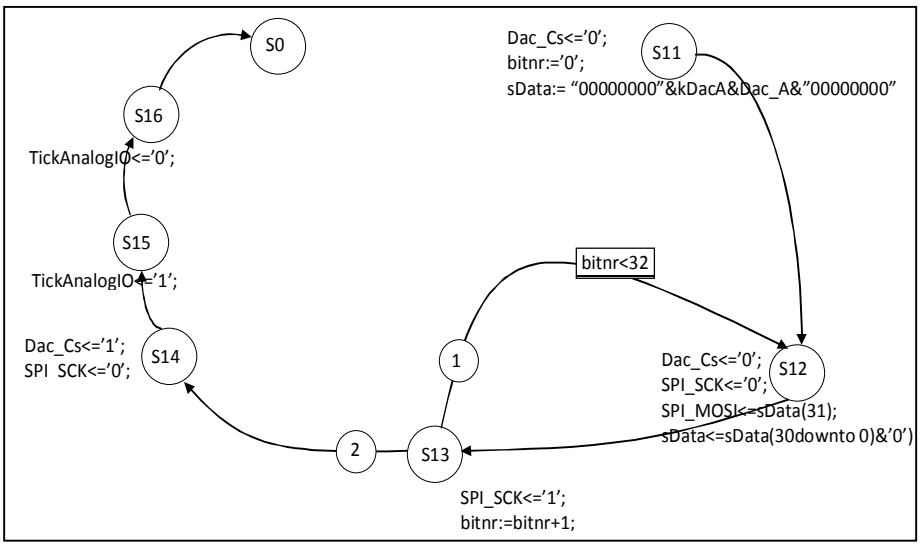

Figure 5. State diagram of FSM for controlling the DAC on board Spatan 3E FPGA Starter kit.

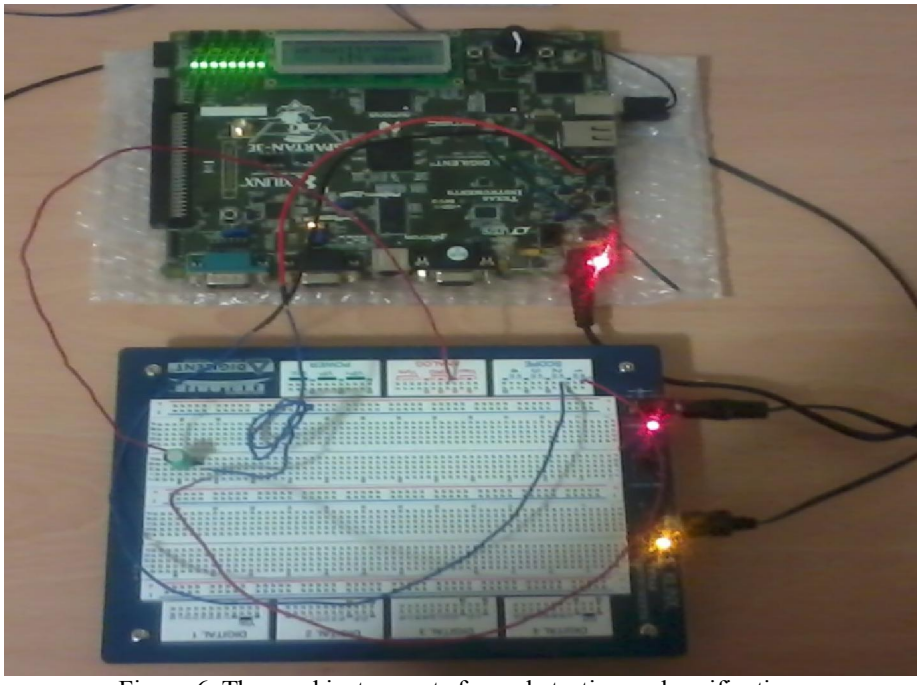

Figure 6. The used instruments for code testing and verification.

3. Verification and Results

The Electronic Explorer board (EE board) has many functions such as Wave-generator, Scope, Digitizer, Multi-meter, programmable-power. The EE board is powered by the free, PC-based WaveForms software that makes it easy to acquire, store, analyze, produce and reuse analog and digital signals. In this work; it was used as a wave generator and scope. The response of the configured FPGA is checked by applying well characterized signals to the input of the amplifier and recognizing their corresponding output signals of the DAC. Many signals from the wave generator on the EE board with amplitudes ranging from 0 - 3.3 V were applied to the input of the amplifier. The applied signal was powered by Waveform software to select the signal type (sinusoidal) and its characteristics (amplitude, offsite and frequency). The gain of the amplifier is set to -1 which is corresponding to voltage range of 0.4 - 2.9 V; it is chosen to allow wide voltage rage that can be sampled. The offset of the signals was adjusted to 1.65 V (corresponding to the reference of the amplifier) and the amplitude of the signals was varied within ±1.25 V. The input signal of the amplifier from the wave

generator and the output signal of DAC are fully characterized by Waveform software that supported to mean of a scope on EE board. Figure 7 illustrates the obtained results of the amplifier input against DAC output for recommended value.

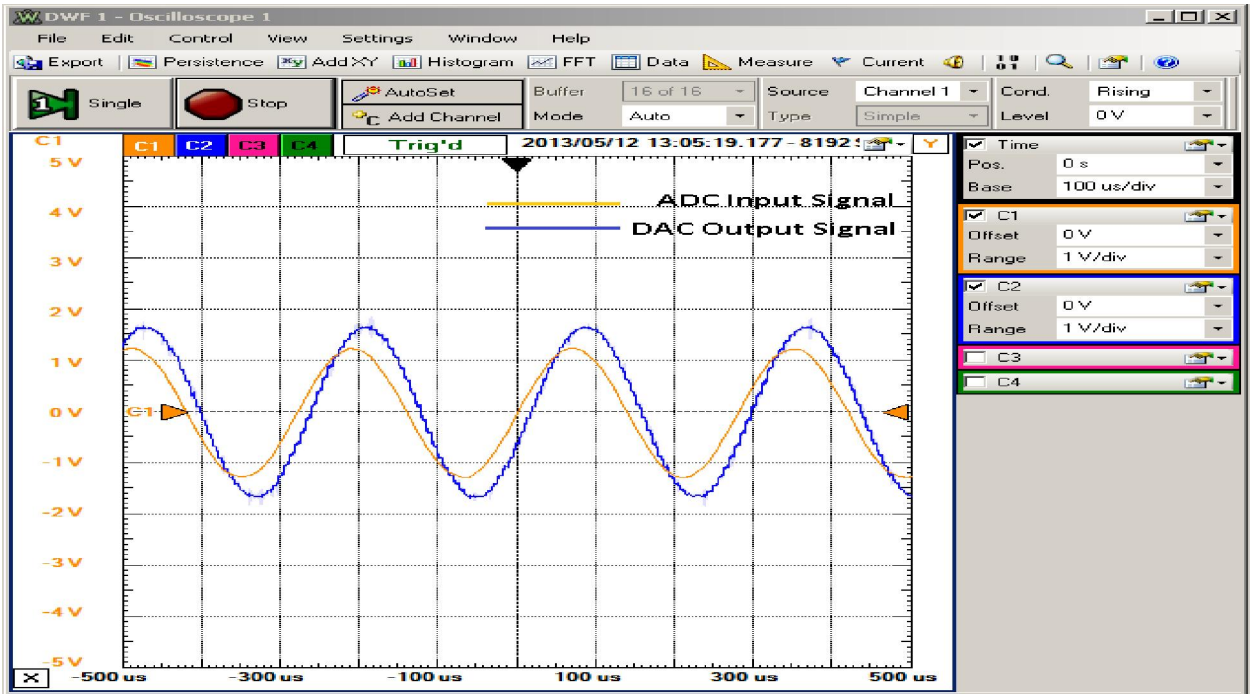

Figure 7. The obtained results of the amplifier input against DAC output for recommended value

As it was expected, the output signal of DAC was matched with the input signal of the amplifier, the amplitude and phase of output signal of the DAC were differ than its corresponding input signal to amplifier. The difference in amplitude is caused due to the differences in both the gain of amplifier and the number of bits of 14-bit ADC and 12-bit DAC as well as the capturing time of the input and output signal i.e. the output signal should be delayed than the input signal because it takes few micro seconds to be generated by DAC. The shape of DAC output was destroyed by changing the values of the offset and amplitude in order to be beyond the recommended values (offset=1.65V, amplitude = ±1.25V) as shown in Figures 8, 9, 10. These figures illustrate the obtained results of the amplifier input against DAC output when raising the amplitude to be (2.31V), raising the offset to be (2.88V) and decreasing the offset value to be (1.81V), respectively. The shape of DAC was not destroyed when using AC coupling capacitor to block DC. Using AC coupling capacitor solve the shape destroying results of the offset change but the amplitude of signal is still limited by the maximum range of the ADC (±1.25V) as shown in figure 11.

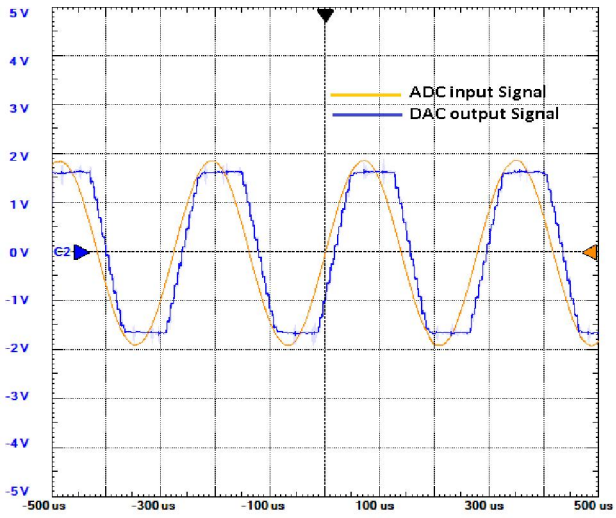

Figure 8. The obtained results of the amplifier input against DAC output when raise amplitude value

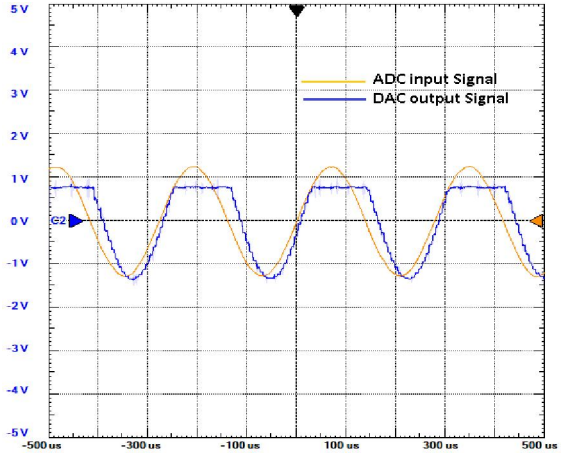

Figure 9. The obtained results of the amplifier input against DAC output when raise offset value

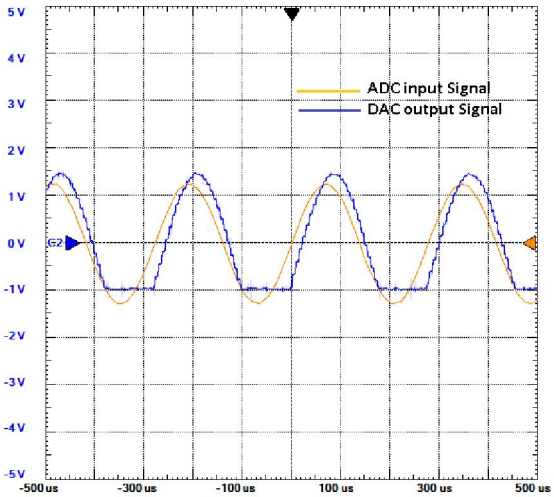

Figure 10. The obtained results of the amplifier input against DAC output when decrease offset value

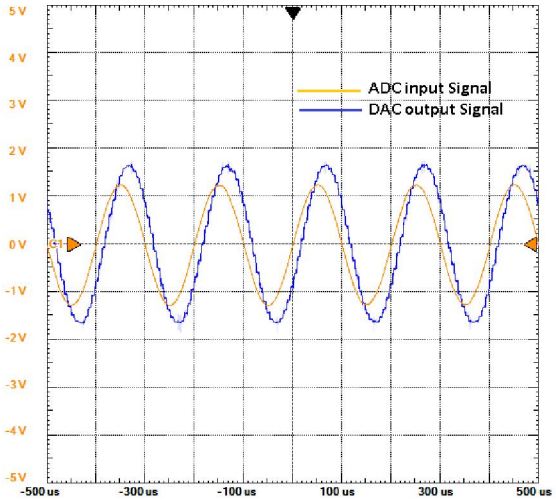

Figure 11. The obtained results of the amplifier input against DAC output using coupling capacitor

4. Conclusion

The controls of amplifier, ADC and DAC of Spartan-3E FPGA Starter Kit board have been applied. The FPGA code was performed through three stages; FSM was implemented for controlling in each component. The results of the implemented VHDL code tends to the on board ADC & DAC of the Spartan 3E FPGA Board were properly interfaced with real world signal.

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