Space Vector Pulse Width Modulation Applied to Three-Level Voltage Source Inverter to Minimize Voltage THD

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Abstract : Multilevel inverters are increasingly becoming an excellent substitution of conventional two-level inverters owing to their superior capability, especially in high-power medium voltage applications. In both types, SVM (Space Vector Modulation) is mostly employed due to its superiority. However the complexity of normal space vector modulation SVM increases sharply with the increased number of level and/or phase of inverters. Multilevel inverters offer several advantages compared to the conventional 3-phase bridge inverter in terms of lower dv/dt stresses, less harmonic components and better output features. This paper presents a three-level Neutral-point-clamped inverter using space vector pulse width modulation SVPWM. The proposed technique target is to have minimum voltage total harmonic distortion THD by selecting the suitable step angle of the PWM vector. PIC18F452 microcontroller is used in the experimental setup for the driving circuit. FLUKE-43X power quality analyzer is used for THD measurment .A simulation model has been designed and verified experiemntally. The results of the phase voltage, line voltage and their harmonics spectrum show a good agreement between the simulation and the laboratory results that have been achieved.
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1. Introduction:

Multilevel inverters have attracted much interest from the researchers especially in applications involving high voltage and high power such as the utility and large motor drive application. This increased recognition of multilevel inverter is due to the limitation of the conventional 2-level inverters in handling high power conversion [1].The multilevel inverter can be developed by either using multiple 3-phase bridges or by increasing the number of switching devices per phase in order to increase the number of levels [2].The concept of multilevel inverter involves in utilizing an array of series switching devices to perform the power conversion in a small increase of voltage steps by synthesizing the staircase voltage from several levels of DC capacitor voltages. The advantage of multilevel inverter are the (dv/dt) stresses on the switching devices are reduced to small increment in voltage steps, reduced electromagnetic interference (EMI) when operated at high voltage, better feature of output voltage in terms of less distortion, lower harmonics contents, lower switching losses, being able to produce seven levels of output phase voltages and five levels of the output line voltage from three different levels of switching signal compared to standard two level inverter [3].As the numbers of levels are increased ,the amount of switching devices and other components are also increased tremendously ,making the inverter becoming more complex and costly. This is one of the disadvantages of multilevel inverters [4]. To control multilevel inverter the pulse width modulation (PWM) strategies are the most effective, especially the space vector pulse width modulation (SVPWM) one, in space vector modulation we have more freedom to choose the sequences of states this freedom choice can be used in order to minimize switching losses, to reduce output ripple or to obtain the input neutral point balancing [5]. In this paper we study a simplification of the space vector pulse width modulation algorism for three levels Neutral-Point-Clamped inverter, the complete computer simulations for three level SVPWM techniques, it also includes practical result for the system to verify simulation results through the result of phase voltage, line voltage and their harmonic spectrum [6].

2. Neutral-Point-Clamped (Npc) Multilevel Inverter

One of the multilevel structures that has gained much attention and widely used is the Neutral-Point-Clamped multilevel inverter or also known as Diode Clamped multilevel inverter. Figure1 shows the three-level NPC inverter. Basically, NPC multilevel inverters synthesize the small step of staircase output voltage from several levels of DC capacitor voltages. An m-level NPC inverter consists of (m-1) capacitors on the DC bus, 2*(m-1) switching devices per phase and 2*(m-2) clamping diodes per phase. Figure 1 shows the structure of three-level NPC. The DC bus

voltage is split into three levels by using two DC capacitors, C1 and C2. Each capacitor has (Vdc/2) volts and each voltage stress will be limited to one capacitor level through clamping diode.The output voltage, V_{AN} has three states as given in Table 1.The number of levels can be extended to a higher level by additional switching devices and with these additions, the inverter will be able to achieve higher AC voltage, producing more voltage steps that will be approaching sinusoidal with minimum harmonics distortion. During inverter operations, the switches near the centre tap are switched on for a longer period compared to the switches further away from the centre tap as given in the switching states in Table 1. As the switch is further away from the centre tap the switching time is shorter. The operation of all the phase groups is essentially identical, consider only the operation of one phase a. Pair of devices with by-pass diodes are connected in series with an additional diode connected between the neutral point and the centre of the pair, as shown in Fig. 1. the devices (T1-a) and (T4-a) function as main devices like a two level inverter, and (T2-a) and (T3-a) function as auxiliary devices which help to clamp the output potential to the neutral point with the help of clamping diodes (D0-a) and (D0-a').Positive phase current i_a will be passed in devices (T1-a) and (T2-a) when the output voltage is positive, by devices (D3-a) when the output is negative, and by devices (D0-a) and (T2-a) at the neutral clamping condition. On the other hand, Negative phase current $-i_a$ will be passed in (D1-a) and (D2-a) when the output is positive, by (T3-a) and (T4-a) when the output is negative, and by (T3-a) and (D0-a') at the neutral clamping condition. This operation gives three voltages levels ($+V_{dc}$, 0 and $-V_{dc}$) at the output phase voltage wave form. The levels of the line voltage wave are $+V_{dc}$, $-V_{dc}$,$+0.5V_{dc}$, $-0.5V_{dc}$ and 0 [7]. The switching states and the operating device are summarized in the Tabl 1.

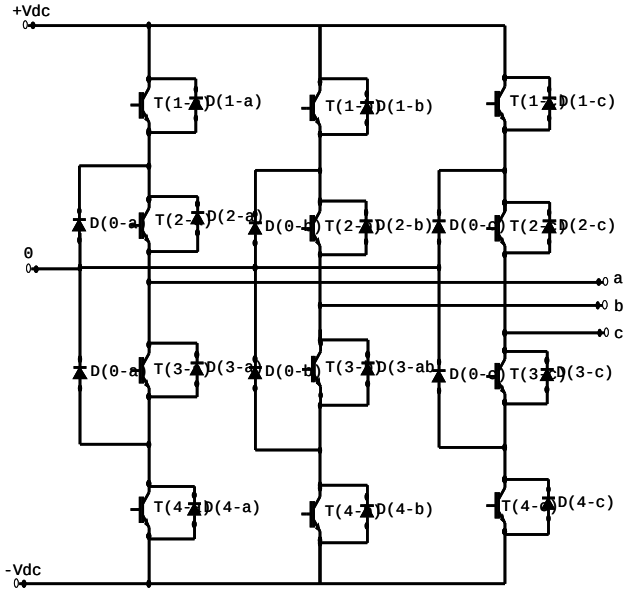

Fig.1: Proposed system power circuit.

Table 1: Switching sequence of phase A.

Switching element				Inverter output voltage	state
T(1-a)	T(1-a)	T(1-a)	T(1-a)		
ON	ON	OFF	OFF	+Vdc	+
OFF	ON	ON	OFF	0	0
OFF	OFF	ON	ON	-Vdc	-

3. Space Vector Modulation

Space Vector Modulation is a technique where the reference voltage is represented as a reference vector to be generated by the power converter. For the operation of three level inverter, there are three switching states for each inverter leg; [P], [O] and [N]. [P] denotes that the upper two switches in leg A are on and the inverter terminal voltage, V_{AN} is +Vdc/2, while [N] means that the lower two switches are on with a terminal voltage of -Vdc/2. Switching state [O] signifies that the inner two switches are on with the terminal voltage equals to zero. There are a total of 27 combination of switching states for NPC inverter. The relation between the switching states and voltage space vectors are shown in Fig. 2.

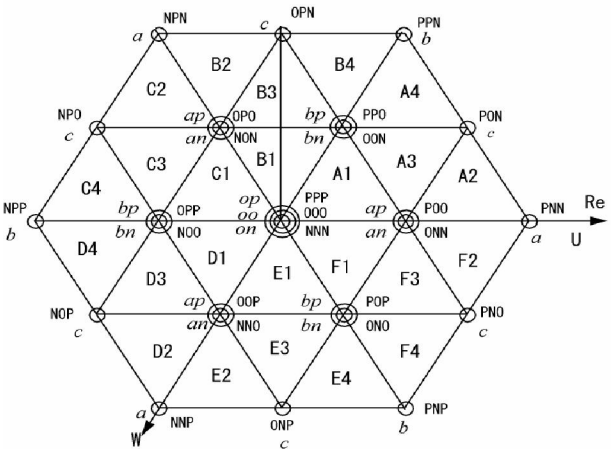

Fig. 2: Space vector hexagon

From the previous space vector diagram we can divide the diagram to six sectors (A, B, C, D, E, and F). Each sector can be divided to four regions as shown in the triangle of sector A as shown in Fig. 3 where;V*=Vdc (phase a is connected to +Vdc, phase b and phase c to –Vdc) [8].

V* = 0.5Vdc (phase a is connected to +Vdc, phase b and phase c to 0 or Phase (a) is connected to 0 phase b and c to –Vdc).

V* =0.866Vdc (Phase a is connected to +Vdc, phase b to 0 and phase c to –Vdc.).

V* =0 (All phases are connected to +Vdc, 0 or –Vdc).

In the space vector PWM, generally, the reference voltage vector is formed by its nearest three voltage vectors in order to minimize the harmonic components of the output phase voltage.

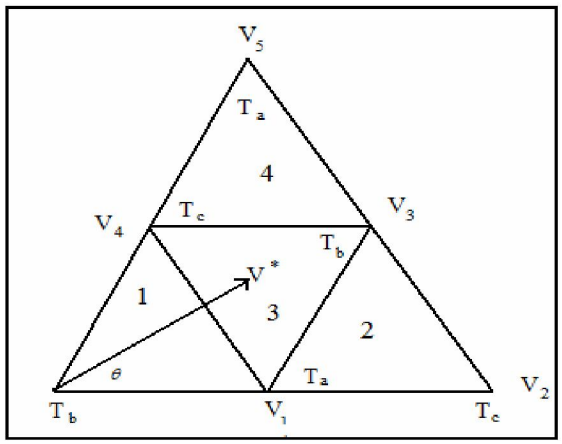

Fig. 3: Sector A (Reg. 1, 2, 3 and 4).

The duration of each voltage vector can be calculated by vector calculation satisfying the following equations assuming the vector passes through the region 1[9].

$$V_1T_a + 0T_b + V_4T_c = V^*\frac{T_s}{2} \quad (1)$$

$$T_a + T_b + T_c = \frac{T_s}{2} \quad (2)$$

Where T_a, T_b and T_c are the respective vector time intervals, and Ts = sampling time. The following equations were derived to calculate the vector duration for T_a, T_b and T_c for the four regions in any sector of the six. Assuming that V* command voltage, V_{dc} = DC link voltage and α is the command voltage vector angle. The proposed vector V* rotating from zero and reaches to angle Θ of 360 degree with N steps depending on the command angle so the step time will be Ts=1/(N* F) where F is the supply frequency. The active space vector equations can be written as follows:

$$v_1 = \frac{1}{2}e^{j\alpha} \quad (3)$$

$$v_2 = 1e^{j\alpha} \quad (4)$$

$$v_3 = \frac{\sqrt{3}}{2}e^{j(\alpha+\pi/6)} \quad (5)$$

$$v_4 = \frac{1}{2}e^{j(\alpha+\pi/3)} \quad (6)$$

$$v_5 = 1e^{j(\alpha+\pi/3)} \quad (7)$$

Region (1) of any sector:

From equation 3, 4,5,6,7 in equation 1, 2, the time equation can be arranged in matrix as follow [10]

$$\begin{bmatrix} T_a \\ T_b \\ T_c \end{bmatrix} = \begin{bmatrix} \frac{1}{2}\cos\alpha & 0 & \frac{1}{2}\cos(\alpha+\frac{\pi}{3}) \\ \frac{1}{2}\sin\alpha & 0 & \frac{1}{2}\sin(\alpha+\frac{\pi}{3}) \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} V^*\frac{T_s}{2}(\cos\theta) \\ V^*\frac{T_s}{2}(\sin\theta) \\ \frac{T_s}{2} \end{bmatrix} \quad (8.1)$$

Region (2) of any sector:

$$\begin{bmatrix} T_a \\ T_b \\ T_c \end{bmatrix} = \begin{bmatrix} \frac{1}{2}\cos\alpha & \frac{\sqrt{3}}{2}\cos(\alpha+\frac{\pi}{6}) & \cos\alpha \\ \frac{1}{2}\sin\alpha & \frac{\sqrt{3}}{2}\sin(\alpha+\frac{\pi}{6}) & \sin\alpha \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} V^*\frac{T_s}{2}(\cos\theta) \\ V^*\frac{T_s}{2}(\sin\theta) \\ \frac{T_s}{2} \end{bmatrix} \quad (8.2)$$

Region (3) of any sector:

$$\begin{bmatrix} T_a \\ T_b \\ T_c \end{bmatrix} = \begin{bmatrix} \frac{1}{2}\cos\alpha & \frac{\sqrt{3}}{2}\cos(\alpha+\frac{\pi}{6}) & \frac{1}{2}\cos(\alpha+\frac{\pi}{3}) \\ \frac{1}{2}\sin\alpha & \frac{\sqrt{3}}{2}\sin(\alpha+\frac{\pi}{6}) & \frac{1}{2}\sin(\alpha+\frac{\pi}{3}) \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} V^*\frac{T_s}{2}(\cos\theta) \\ V^*\frac{T_s}{2}(\sin\theta) \\ \frac{T_s}{2} \end{bmatrix} \quad (8.3)$$

Region (4) of any sector:

$$\begin{bmatrix} T_a \\ T_b \\ T_c \end{bmatrix} = \begin{bmatrix} \cos(\alpha+\frac{\pi}{3}) & \frac{\sqrt{3}}{2}\cos(\alpha+\frac{\pi}{6}) & \frac{1}{2}\cos(\alpha+\frac{\pi}{3}) \\ \sin(\alpha+\frac{\pi}{3}) & \frac{\sqrt{3}}{2}\sin(\alpha+\frac{\pi}{6}) & \frac{1}{2}\sin(\alpha+\frac{\pi}{3}) \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} V^* \frac{T_s}{2}(\cos\theta) \\ V^* \frac{T_s}{2}(\sin\theta) \\ \frac{T_s}{2} \end{bmatrix} \quad (8.4)$$

The resultant time intervals are distributed accordinally to generate symmetrical PWM pulses with neutral point voltage balancing.

4. Proposed Svpwm Algorithm

- Ø Calculate the switching time at certain switching frequency Ta, T_b and Tc.
- Ø To avoid extra switching transitions, when moving between triangles at the same sector from region to the next, the correct switching sequence for the switching period should be also identified that means only one status for each phase has to be changed than the previous region.
- Ø Generate the switching pattern according to the switching sequence in Table 2.
- Ø Each switching pattern during Ts/2 is repeated inversely in the next Ts/2 interval with appropriate segmentation of Ta, T_b and Tc intervals in order to generate symmetrical PWM waves to reduce harmonics effects as shown in Fig. 4.
- Ø Calculate THD at constant modulation depth equal to 0.866 for each step angle according to equation 9.

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} V^2_{anh}}}{V_{an1}} \quad (9)$$

Where; h is the harmonics order and V_{an1} is the magnitude of fundamental phase voltage.

- Ø Calculating the THD at different step angle to have the optimum angle that has minimuim THD.
- Ø The results are listed in Table 3 shows the summery of the THD at different step angles.

Table 2: The proposed switching sequence of phase A

Sector	phase	Region 1	Region 2	Region 3	Region 4
A	a	N000PPP	0PPP	00PPP	0PPP
	b	NN000PP	NN00	N000P	00PP
	c	NNN000P	NNN0	NNN00	NNN0
B	a	PP000NN	PP00	P000N	00NN
	b	PPP000N	PPP0	PPP00	PPP0
	c	P000NNN	0NNN	00NNN	0NNN
C	a	NNN000P	NNN0	NNN00	NNN0
	b	N000PPP	0PPP	00PPP	0PPP
	c	NN000PP	NN00	N000P	00PP
D	a	P000NNN	0NNN	00NNN	0NNN
	b	PP000NN	PP00	P000N	00NN
	c	PPP000N	PPP0	PPP00	PPP0
E	a	NN000PP	NN00	N000P	00PP
	b	NNN000P	NNN0	NNN00	NNN0
	c	N000PPP	NPPP	00PP	0PPP
F	a	PPP000N	PPP0	PPP00	PPP0
	b	P000NNN	0NNN	00NNN	0NNN
	c	PP000NN	PP00	P000N	00NN

Where: N = -ve state, 0 = zero state and P = +ve state.

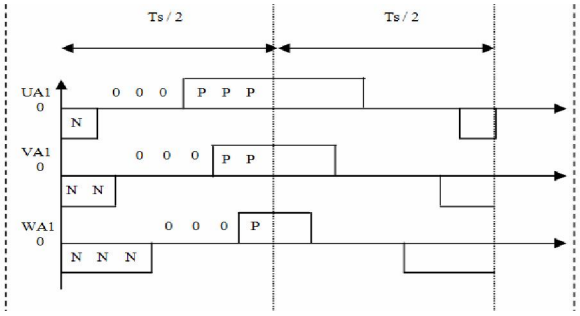

Fig .4: Symmetrical switching pattern of three phases for two consecutive Ts intervals of region 1 in sector A.

Table3:THD at different step angle

Step angle	THD
45	19%
30	15%
15	8%
7.5	3.9%

5. SIMULATION RESULTS AND DISCUSSIONS

The simulation of proposed system were done by using MATLAB / SIMULINK to simulate neutral point clamped inverter driven by SVPWM The result includes the switching signal, phase voltage, line voltage, and the harmonic spectrum of the phase and line voltage swept for thirty orders of harmonics. Figure 5 shows the schematic diagram of the proposed system and includes the power circuit that has single phase uncontrolled, filter capacitors, three level inverter and voltage measurements. NPC output phase and line voltages wave forms at step angle 7.5 degree and switching frequency 2400 HZ are shown in Figures from (6.a to 6.f). These figures show four cycles for the inverter output voltages which are symmetrical and has a phase shift 120 Degree and also the fundemental frequency is 50 Hz .The calcualted total harmonic distortion THD for phase a voltage is indicates at Fig. 7 . Its value is 3.5% which is suitable for all type of drive applications.

Table 4: Simulation data

Dc bus voltage	300volt
Switching frequency	2400hz
Sampling time Ts	$4.16*10^{-4}$
Modulation depth	0.866
Vector Step angle	7.5 degree

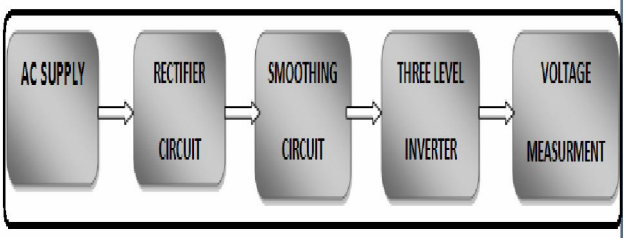

Fig.5: Schematic diagram of the proposed system

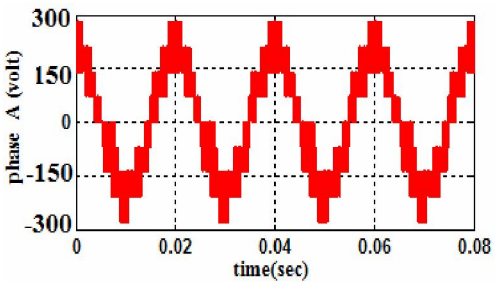

Fig .6.a: The voltage wave form of phase A

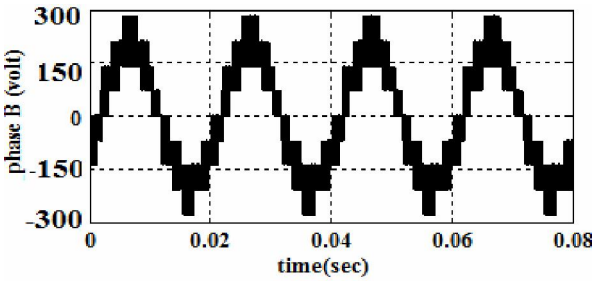

Fig .6.b: The voltage wave form of phase B

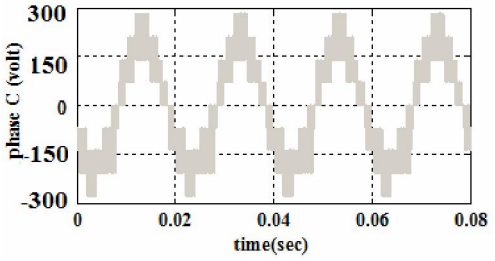

Fig .6.c: The voltage wave form of phase C

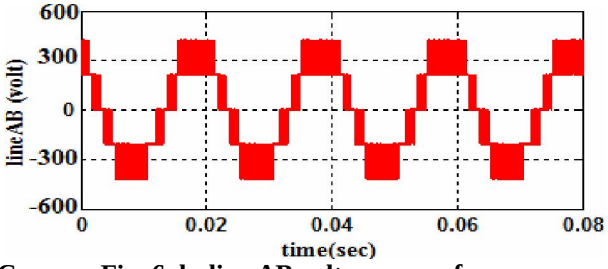

Fig .6.d: line AB voltage wave form

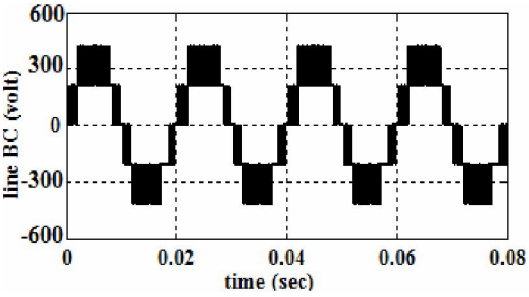

Fig .6.e: line voltages B C wave form

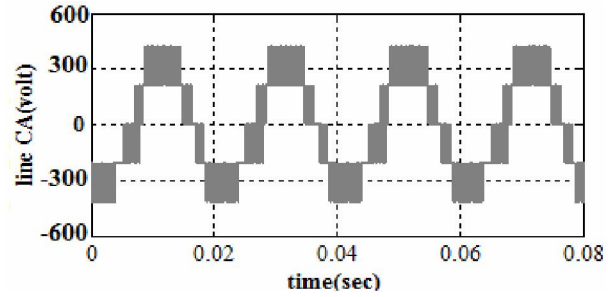

Fig .6.f: l line voltages CA voltage wave form

Fig.6: Simulation phase and line voltages wave form at step angle 7.5 degree

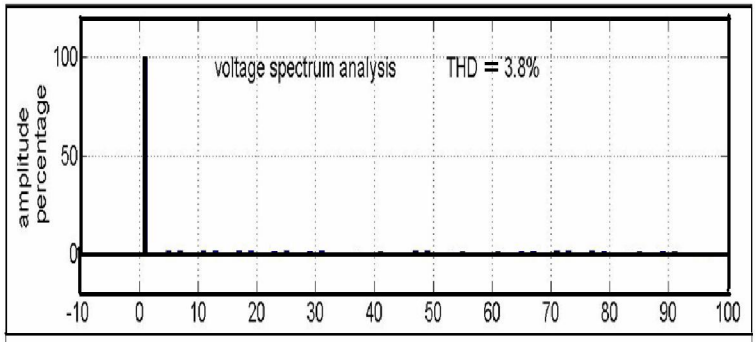

Fig .7: THD spectrum for phase voltage A

6. Hardware Implementation

The block diagram of the proposed system is shown in Fig. 13 Presents the practical implementation of the equipment to operate three-level neutral points clamped using SVPWM. This control choice implemented using PIC18F452 Microcontroller. The figure includes the power circuit that has single phase uncontrolled rectifiers, isolated transformer, two filter capacitors, three level inverter, 12 unit of isolating circuits using 4N35 opt-coupler isolator, 12 units of delay circuits using 74LS121 with 74LS08 logic gate, measurement of voltage and PIC18F452 kit of microcontroller as a driving circuit. NPC experimental output phase voltages at step angle 7.5 degree and switching frequency 2400 HZ. The schematic diagram of the expeimental setup is shown in Fig.8. The three phases and line voltages are shown in Figures from (9.a- 9.f) . These figures show measurments of four cycles for the inverter output voltages using FLUKE 43X power quality analyzer. The three phase voltages are symmetrical and have a phase shift 120 Degree and also the fundemental frequency is 50 Hz .The measured total harmonic distortion THD for phase a voltage is indicates at Fig. 10 . Its value is 3.5% which is suitable for all type of drive applications . THD value in both experimental measurment and the simulation calculated value is equal that is verifying the simulation model.

The expeimental total harmoics distorsion THD at angle equal 7.5 degree for the three phase voltages is indicates in Fig.10, its valuse is 3.8% which agreed and verify the simulation model results.

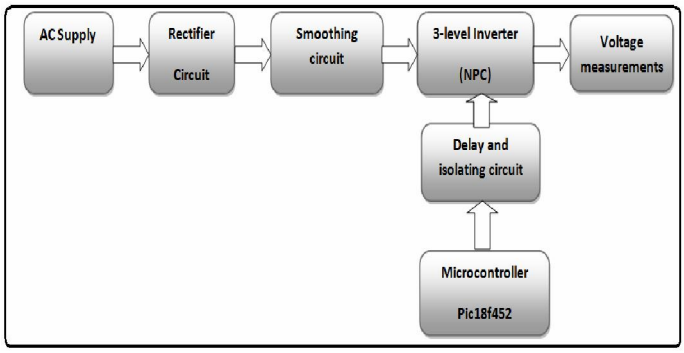

Fig .8: Schematic diagram of the experimental system

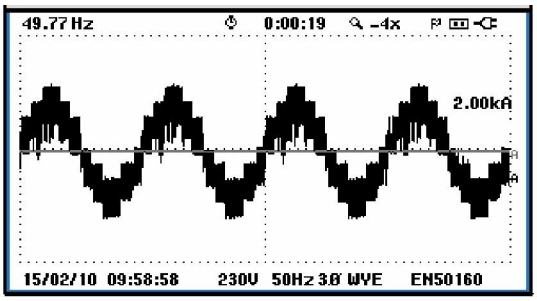

Fig .9.a: Experimental phase voltage A wave form

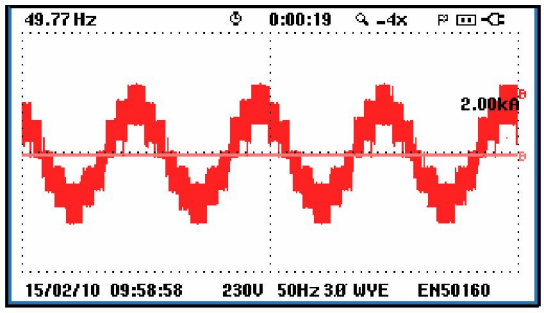

Fig .9.b: Experimental phase voltage B wave form

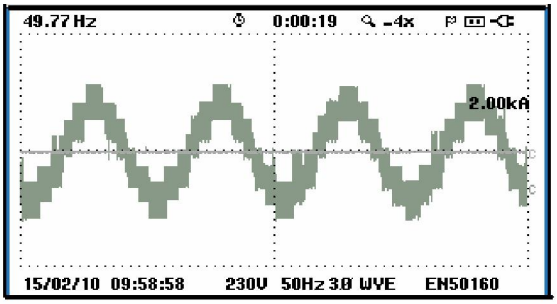

Fig .9.c: Experimental phase voltage C wave form form

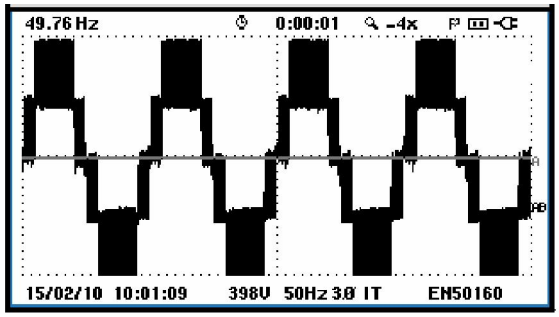

Fig.9.d: Experimental line voltage A&B wave

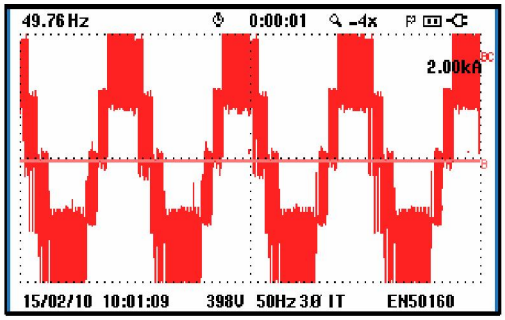

Fig.9.e: Experimental line voltage B&C wave form wave form.

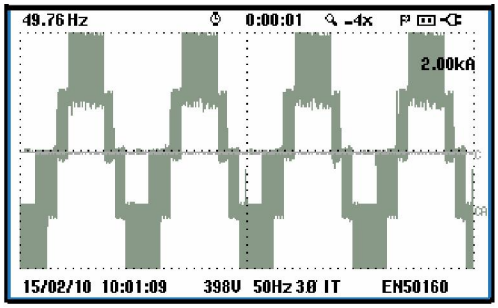

Fig.9.f: Experimental line voltage C&A

Fig.9: Experimental three line voltage wave forms

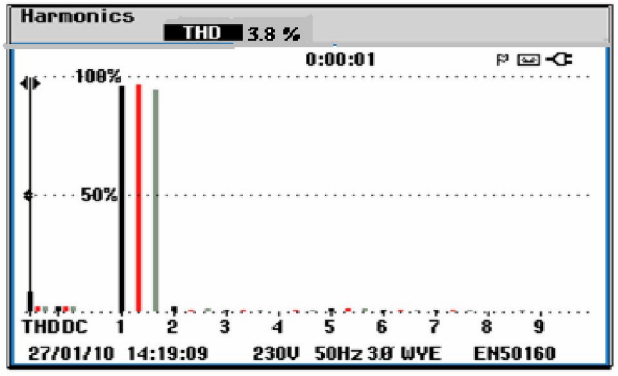

Fig. 10: Expeimental THD Harmonics spectrum for three phase voltage.

7. Conclusion

In this paper, a simulation model and experimental work concerning the application of the SVPWM control strategy applied to three-level voltage inverter were presented. This last aimed on the one hand to prove the effecteness of SVPWM in the contribution of the switching power losses reduction, and to show the advantage of multi-level inverters that carry out voltages with less harmonics content's injection. The coherence between simulation and experimental results confirms the validity of the study.

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