Characterization and Output Characteristics of Al (6 mol %) Doped $PbTiO_3$Thin Film Transistors

May Aye Khaing[1], Than Than Win[*2], Yin Maung Maung[1] and Ko Ko Kyaw Soe[3]

[1]Department of Physics, University of Kyaingtong, Myanmar
[*2] Department of Physics, University of Yangon, Myanma, [3]Pro-Rector, Yangon Institute of Education, Myanmar
mayayekhaing12450@gmail.com, thannthannwinn@gmail.com, dryinmgmg@gmail.com,dr. kokokyawsoe@gmail.com

Abstract: Al doped $PbTiO_3$ powder was firstly prepared by high temperature solid state reaction route. Structural and microstructural properties were studied by X-ray diffraction (XRD) and scanning electron microscopy (SEM)).Fabrication mechanism of a single-transistor type ferroelectric field effect transistor (1TFeFET) memory with $PbTi_{(1-x)}Al_{(x)}O_3$ (PTA) film was prepared by non-expansive and unsophisticated techniques. Electric characteristics (drain & transfer) of all films were measured. The FeFET with PTA6 at 600°C exhibited the smallest value of threshold voltage (3.33V). The mth power of PTA6 cell at 500°C indicated the most suitable for parabolic behaviour. According to the experimental results the laboratory-prepared transistors were utilized for 1T of non volatile ferroelectric random access memory (NVFRAM).
[May Aye Khaing, Than Than Win, Yin Maung Maung and Ko Ko Kyaw Soe. **Characterization and Output Characteristics of Al (6 mol %) Doped $PbTiO_3$Thin Film Transistors.** *Researcher* 2014;6(3):15-20]. (ISSN: 1553-9865). http://www.sciencepub.net/researcher. 3

Keywords: XRD, SEM, 1TFeFET, PTA

1. Introduction

The nonvolatile memory is a memory which retains store data even its external power supply is disconnected [1]. Nonvolatile is divided into ROM (Read-only-memory) that can be read and RAM (random-access memory) that can be read and written [2]. FRAM is a type of ferroelectric random access memory that uses a ferroelectric thin film. That is a promissing candidate for nonvolatile memory [3].

Recently there is an increasing interest in co-existence of the ferroelectricity and ferromagnetism of multiferronics has wide range of new applications including spintronics [4], new data-storage media and multi-state memories [5]. Ferromagnetism and ferroelectricity originate from local spins and off center structured distortion, respectively [6].

For the past two years, FRAMs have attracted much attention due to their potential advantages such as nonvolatility, unlimited write cycles and low power consumption [7]. Perovskite-phase metal oxide exhibit a variety of interesting physical properties and piezoelectric behavior [8]. Perovskite type lead titanate ferroelectric thin films have been demanded for application to many kinds of electric devices, such as capacitors, actuators and transducers. However the degradation of ferroelectric properties with decreasing film thickness is a common problem of $PbTiO_3$ type ferroelectric thin films. This degradation is caused mainly by oxygen vacancies that diffused from the film surface through the grain boundaries during firing [9] [10]. In order to improve the electric properties of the complex $PbTiO_3$ ceramics, a lot of elements have been doped one of the present authors have reported that Al substituted to Ti since the radius of Al^{3+} cat-ion is about the same as that of Ti^{4+}, and found that the Al doped $PbTiO_3$ thin films showed low leakage current as compared with $PbTiO_3$ thin films [11].

Today, ferroelectric memories are moving from the laboratory to the market place. FRAM with one transistor and one capacitor (1T1C) per cell has been used for commercial applications [12]. Nondestructive read out (NDRO) FRAM which has a transistor as a memory cell has high attention since the ferroelectric gate offers simpler circuits and excellent performance [13].

2. Experimental Procedure

To prepare the colloidal precursor solution, PbO, TiO_2 and Al_2O_3were used as starting materials. The purity of materials was 99.9% as Aanalar grade. Each chemical was ground in agate mortar for 3 h to form homogeneous grain size. To reduce the grain size, the powder was sieved with 3-stages mesh sieve (100 mesh, 250 mesh and 400 mesh). Then this sample powder was dispersed by the air-jet milling under the pressure of 40 lb/in^2 to obtain the moisture less particle and blander for 15 min with constant pressure to ensure good dispersion. And then the powder was ground by ball-milling in 20 h. Then they were mixed to get the chemical formula $PbTi_{(1-x)}Al_xO_3$ (x=0.06mol). And then it was heated at 800°C and 900°C for 1 h. The PTA powder (900°C) was chosen for further investigation because of its smaller crystallite size. Al doped $PbTiO_3$ were weighed and

dissolved in 2 methoxyethanol solvent. The mixture solution was acidified with 3 mg of HCl. The solution was stirred and refluxed to form precursor solution.

The substrate used for this study was p-Si(100), which were(0.5cm×1cm) and thickness of 280-300 μm. Before film fabrication, they were washed ultrasonically in distilled water. Then they were washed in boiling acetone and in boiled propenol for 5 min to remove greasy films. And then they were immersed in nitric acid for 5 min in order to remove ionic contamination. After that they were etched in buffered hydrofluoric acid for 5 min to remove oxide films. Finally the Si wafers were cleaned in distilled water and dried on flat oven at 100°C in open air for a few minutes then the cleaned Si wafers were obtained.

SiO_2, as an insulating layer, was thermally deposited on p-Si (100). The middle zone of SiO_2/Si structure was covered with apiezon wax and the remaining zones were etched with HF: DI water (1:3) to remove SiO_2 layer totally. To fabricate source (S) and drain (D) regions, n type phosphorus was deposited on these layers and annealed at 550°C for 1 h.

By diffusion mechanism, S and D regions were formed at the ends. And then, the precursor solution was deposited on middle zone of SiO_2 layer using spin coating to get gate region. The three process temperatures (500°C, 600°C and 700°C) were also performed according to examine the PTA film quality at different annealing temperature. Figure 1 showed fabrication and deposition procedure of MFIS field effect transistor.

3. Results

A. XRD Analysis

The information about the crystallographic properties such as crystallite size and lattice parameters of the samples were examined by XRD profiles. The XRD spectra of $PbTiAlO_3$ powder with different reaction temperatures at 800°C and 900°C were shown in figure 2 (a & b). As shown in Fig,the XRD spectrum of PTA powder graphs were produced within the diffraction angle range from 10° to 70°.The dominant peaks were formed at(101) plane with 2 θ 31.90° and 31.96°, respectively. The lattice parameters, FWHM, and crystallite size (G) were listed in Table 1. From XRD profiles, Al-ion was successfully occupied by Ti-site of $PbTiO_3$ lattice at both temperatures.

B. SEM Analysis

SEM investigation was performed to study the grain morphology of PTA powder at different annealing temperatures. Figure 3 (a & b) showed the SEM image of PTA powder at 800°C and 900°C. The powder was composed by spherical shaped densely packed particles. The grain arrangement was seemed to be uniform and crack free. The grain-size of PTA powder was estimated to be 0.643 μm at 800°C and 0.5 μ m at 900°C.

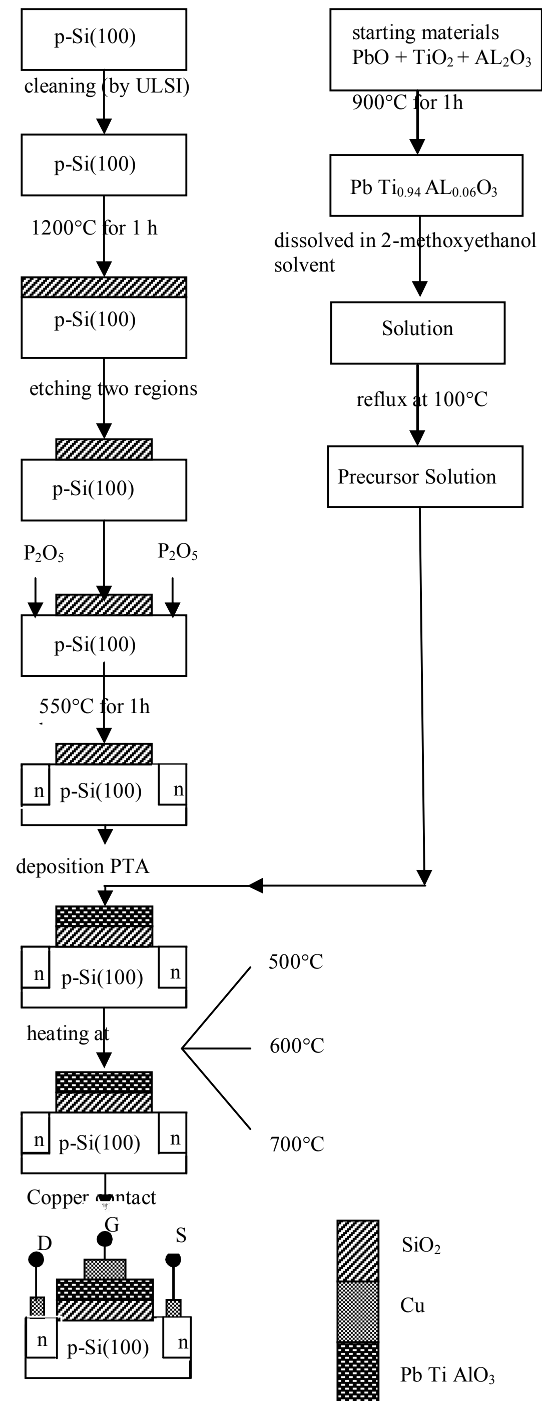

Figure 1 Fabrication and deposition procedure of FeFET

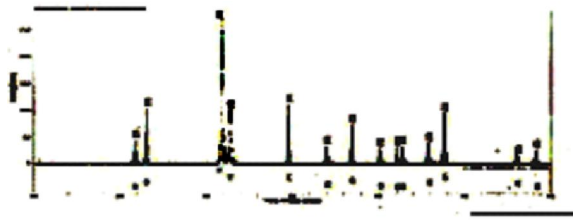

Figure 2(a) XRD pattern of $PbTiAlO_3$ powder at 800°C

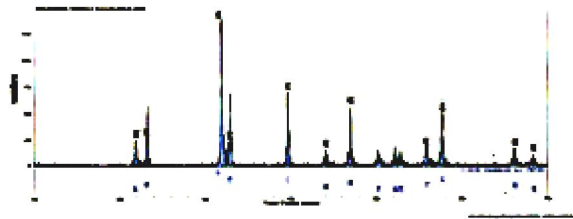

Figure 2(b) XRD pattern of $PbTiAlO_3$ powder at 900°C

Table 1. Structural properties of $PbTiAlO_3$ powder

Process Temperature (°C)	800	900
a - axis(Å)	3.8559	3.8559
c - axis(Å)	4.0703	4.0693
c/a	1.0556	1.0556
FWHM (rad)	2.69E-3	4.05E-3
Crystallite size (nm)	52.5	38.8

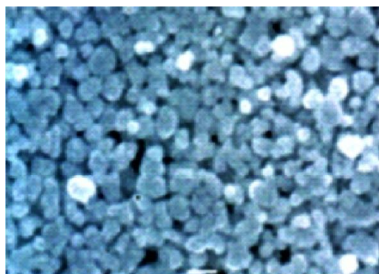

Figure 3(a) SEM image of $PbTiAlO_3$ powder at 800°C

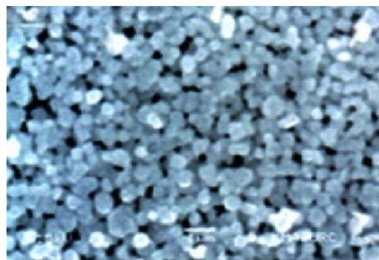

Figure 3(b) SEM image of$PbTiAlO_3$ powder at 900°C

C. Output Characteristics

To examine the output characteristics of fabricated transistor, I_{DS}-V_{DS} variation (drain characteristics) was measured at different gate to source voltages. The characteristic curves were displayed at figure 4(a-c). From the figure, it was found that two different regions such as linear and saturation were observed.

At low drain voltage, between 0V to 4V, the drain current increased linearly with increase in drain voltages. In this region, the FET exhibited a resistive characteristics with the resistance as a function of the gate voltage. The drain current I_D increased with increase in drain voltage V_D and become saturated at the pinch-off point. After that, the I_D did not increase whereas increased in drain voltage V_D, which showed saturated or constant region.

Moreover, the drain current was also enhanced with increasing gate voltages. So transistor fabricated was only operated in E-mode(enhancement-mode).

From drain characteristic curve, the drain current did not allowed to flow when the drain voltage approached zero. On the other hand, the drain current was zero if zero-bias gate voltage was applied. These facts showed the fabricated FeFET had normally- off nature.

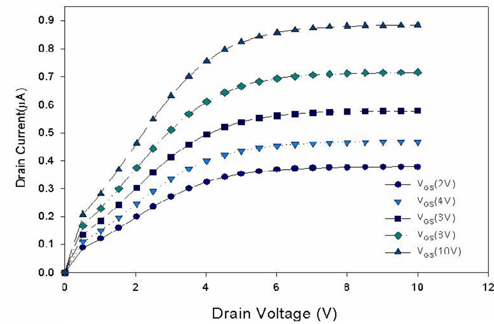

Figure4 (a) Drain characteristic of PTA-gated FET at 500°C.

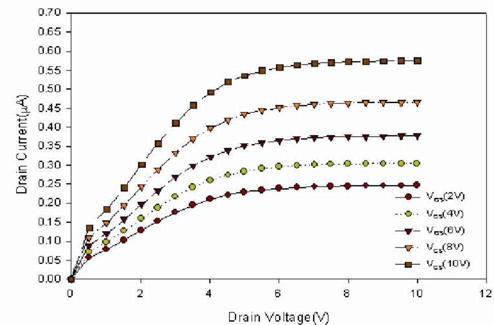

Figure4 (b) Drain characteristic of PTA-gated FET at 600°C.

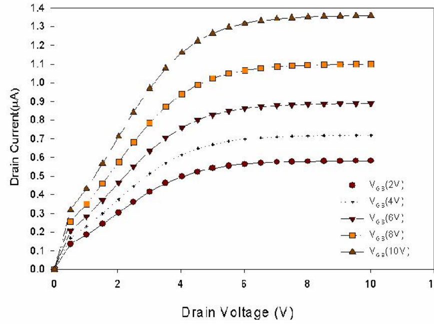

Figure 4 (c) Drain characteristic of PTA-gated FET at 700°C.

To examine the device quality, (I_{DS}-V_{GS} variation), transfer characteristics were essentially observed at saturation-mode. These graphs were shown in figure 5 (a-c). From the figure, it was seen that the I_{DS} was exponentially increased with gate voltage.

All transfer curves were varied gate potential with threshold voltage. All threshold voltages were found to be temperature influence and these were listed in Table.2.

The largest maximum drain current was caused by the cell at 700°C. To check the parabolic nature of transfer curve (or) the I_{DS} and (V_{GS} -V_{TH}) variation, m^{th} power of

(V_{GS} -V_{TH}) was essentially studied by two unknown equations

$I_{DS} = K (V_{GS}-V_{TH})^m$

Where I_{DS}= drain current

K= constant

V_{GS}= gate to source voltage

V_{TH}= threshold voltage

At V_{GS} = 6V, V_{TH} = 3.44 V, I_{DS} = 5.6 μA

V_{GS} = 7V, V_{TH} = 3.44 V, I_{DS} = 11 μA

$5.6 = K (6 - 3.44)^m$ (1)

$11 = K (7 - 3.44)^m$ (2)

Eqn (2) / (1),m =2.04 for the cell at 500°C. The mth power values were collected in Table.2.

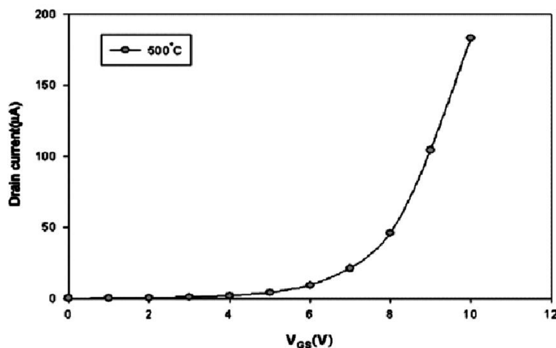

Figure 5 (a) Transfer characteristics of PTA-gated FET at 500°C

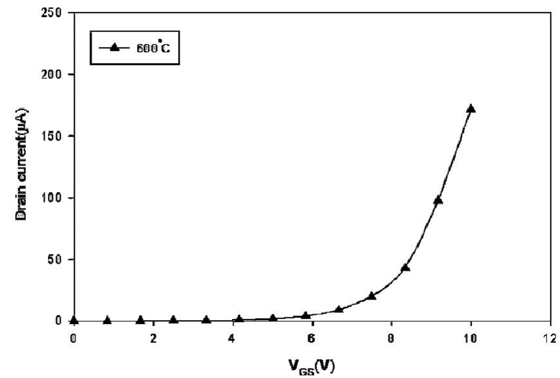

Figure 5 (b) Transfer characteristics of PTA-gated FET at 600°C

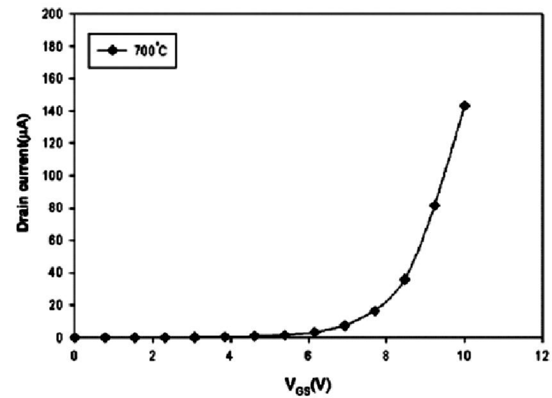

Figure 5 (c) Transfer characteristics of PTA-gated FET at 700°C

To identify the transconductance value, $I_D^{1/m}$ was characterized with V_{GS} and shown in figure 6 (a-c). From the characteristic curve, $I_D^{1/m}$ was linearly enhanced when the gate to source voltage was increased. The slope gave its transconductance value. The g_m value was measured by equation $g_m = \Delta I_D / \Delta V_{GS}$. A large transconductance was desirable to minimize the gate drive and provided high power gain. These values were organized and quoted in Table 2.

Table 2 V_{TH}, $I_{D,max}$, m^{th} power and g_m at different process temperatures

Process Temperature(°C)	500	600	700
V_{TH}(V)	3.44	3.33	4.33
I_{Dmax}(μA)	0.57	0.88	1.37
m^{th} power	2.04	1.95	2.11
g_m(μS)	1.7561	1.4853	2.4405

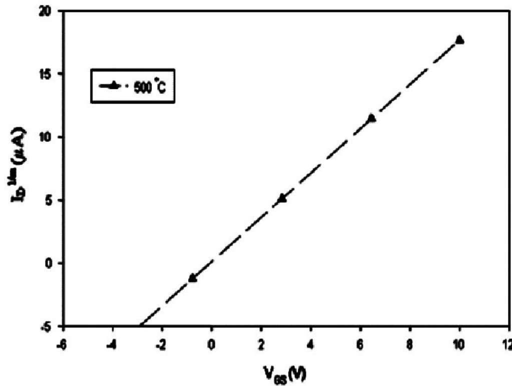

Figure 6 (a) Transconductance characteristics of PTA gated FET at 500°C
in saturation mode.

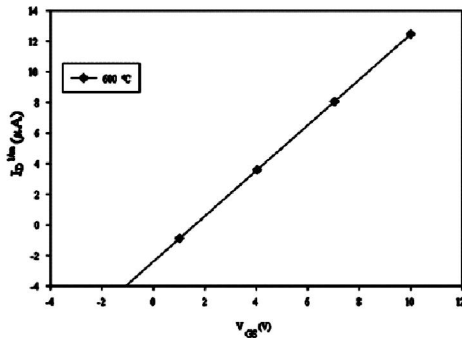

Figure 6 (b) Transconductance characteristics of PTA gated FET at 600°C
in saturation mode.

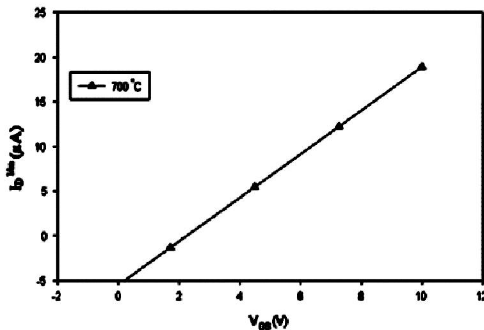

Figure 6 (c) Transconductance characteristics of PTA gated FET at 700°C
in saturation mode.

4. Discussion

Fabrication of PTA 6 gated FET and its output characteristics had been studied. According to the experimental results, salient conclusions were made as follows. The fabricated cells were only operated in E-mode. The normally-off nature of fabricated cells was found on drain characteristic curve too.

From transfer characteristics, I_{DS} and V_{GS} graph was found to be parabolic nature as $I_{DS} = K (V_{GS}-V_{TH})^2$. $I_D^{1/m}$ and V_{GS} graph was examined to be linear relationship. The measurement m^{th} power values were ranged from 1.95 to 2.11. This fact gave the parabolic nature of transfer curve for fabricated cells. The slope of $I_D^{1/m}$ - V_{GS} graph gave the transconductance value of fabricated cells. According to the experimental results such as threshold voltage, m^{th} power, and transconductance values, the laboratory-prepared transistor can be utilized for 1T of NVFRAM.

Acknowledgement

This research work was fully supported by Department of Physics, University of Yangon, Myanmar.

Corresponding Author:
Dr Than Than Win
Department of Physics,
Yangon University
E-mail: thannthannwinn@gmail,com.

Authors' and References' Information

1. Name: Dr May Aye Khaing (Assistant Lecturer) Kyaing tong University, Myanmar Office Address: Department of Physics, Kyaingtong University, Myanmar Phone:+51-095086838
2. Name: Dr Than Than Win (Lecturer) University of Yangon, Myanmar Office Address: Department of Physics, University of Yangon, Myanmar Phone:+51-095059602
3. Name: Dr Yin Maung Maung (Lecturer) Kyaingtong University, Myanmar Office Address: Department of Physics, Kyaingtong University, Myanmar Phone:+51-0973084418
4. Name: Dr Ko Ko Kyaw Soe (Pro-Rector) Yangon Institute of Education, Myanmar Phone: +51-09448026411
5. Dr Thet Naing Oo (Post Doctoral Researcher) Nagaoka University of Technology Department of Electrical Engineering Email: tnaingoo@gmail.com. Tel:+81-258-47-1611(Ext 5321).
6. Dr Tin Aung, Professor and Head (Rtd), Department of Physics, University of Yangon Email: mintha.7@gmail.com

References

1. Magalani V, Agnihotri A, " Remanent Polarized Ferroelectric Non-volatile Random Access Memory, " International Journal of Recent Research and Review.1,(2012),16-21.
2. Bez R, Pirovano A, " Non-volatile memory technologies: Emerging concepts and new

materials", Materials Science in Semiconductor Processing, 7, (2004), 349-355.
3. Yoon S.M, Tokumitsu E and Ishiwara H.," Improvement of Memory Retention Characteristics in Ferrorelectric Neuron circuits using a Pt/ $SrBi_2Ta_2O_9$ / Pt / Ti / SiO_2 / Si Structure Field Effect Transistor as a Synapse Device." Jpn .J .Appl .phys, 39, (2000), 2119-2124.
4. Fiebig M, Lottermoser T, Frohlich D . Gottsev AV & Pisarev RV, " Room temperature maganeto electric control of micro maganetic structure in iron gamet films." Nature, 419 (2002) 818.
5. Spaldin NA & Fiebig M, " The Resistance of Magnetoelectric Multiferronic Science." 309 (2005) 391-392.
6. Hemberger J, Lunkenheimer P, Fichtl R, Krugvon N.H.A, Tsurkan V and Loidl A, "Multiferronic properties of $Pb_2Fe_2O_5$ ceramics materials, " Nature, 434 (2005) 364-367 ; 19.
7. Saif AA, Jamal ZAZ, Sauli Z, & Poopalan P, " Fabrication and Electrical Characterization of Al / Ba_x Sr_{1-x} TiO_3 / Pt / SiO_2 / Si Configuration for FeFET Applications, "World Academy of Science, Engineering and Technology 57 (2011) 14-17.
8. MaO Y, Zhou H, & Wong SS, "Synthesis, Properties, and Applications of Perovskite-Phase Metal Oxide Nanostructures, " Materials Matters (2010), 5.2, 50, 1-8.
9. Iijima T, Sanada N, "Ferroelectric Properties of Sol – Gel – Derived $PbTiO_3$ Type Thin Films, " Jpn.J.Appl. Phys, 35, (1996), 4930-4932.
10. Iijima T, kudo S, Sanada N, "Effect of Film Thickness on Ferroelectric Properties of Sol – Gel – Derived Pb (Ti, Al)O_3 Thin Films, " Jpn.J.Appl.Phys, 36, (1997), 5829-5833.
11. Zhang BP, Li JF, Dong Y, & Iijima T, " Electrical and Physical Properties of Al and Nb Doped $PbTiO_3$ Ceramic Thin Films," Materials Science Forum vols. 457-479 (2005), 1587-1590.
12. Lin CM, Shin W,Chang IY,.Juan PC, &Lee JV, " Metal Ferroelectric ($BiFeO_3$) insulators (Y_2O_3)-semiconductor capacitors and field effect transistors for non-volatile memory applications," Appl. Phys. Lett. 94, 142905, (2009), 1-3.
13. Saif AA, Jamal ZAZ, Poopalan P, " Effect of the chemical composition at the memory behavior of Al / BST / SiO_2 / Si – gate – FET structure," Appl Nanosci (2011) 1:175-162.

3/5/2014