Low Voltage Tunable Square-Root Domain Band-Pass Filter with Translinear Loop Technique in Biomedical Engineering

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Received February 2, 2008

Abstract

A low voltage square root domain filter based on the MOSFET square law is proposed in this thesis. Through HSPICE simulation, the extendibility and the reliability of the design procedure are verified. Furthermore, the supply voltage is successfully reduced down to 0.9V by the Flipped Voltage Follower (FVF) low-voltage technique without regarding the performance of the filters. The proposed filter structure has the merits of low-power voltage supply operation, high frequency operation, and the wide range of pole frequency tuning capability. The proposed circuit has been simulation with the TSMC 0.18 μm CMOS technology. The experimental results have demonstrated that the center frequency f0 of the band-pass filter can be electronically tunable in 774-914kHz with tunable bias-current, 1.78% total harmonic distortion (THD), and the power dissipation is less than 387μW at a 0.9V supply voltage. [Life Science Journal. 2010; 7(1): 30 – 33] (ISSN: 1097 – 8135).

Key Words: translinear loop; flipped voltage follower; square-root domain; band-pass filter; current-mode circuit

1. Introduction

Recently, there is a growing interest in the field of translinear filters. Main advantages of regarding to these various filters are large dynamic range and low-voltage/low power operation capability. Since the voltage swings of internal capacitors are compressed, DC power supply voltage will be less restrictive to the maximum input signal. Initially, a subclass of translinear filters was the log-domain filters introduced by Adams [1]. On the other hand, a subclass of translinear filters, named "square-root domain filter" was introduced. Toumazou[2] proposed state-space synthesis of the second filter which was the first filter structure using the MOSFET square law. Although an alternative biasing of MOS translinear loops based on the application of the Flipped-Voltage Follower (*FVF*) was proposed[3-5], it allowed a significant reduction in the voltage supply requirements. In order to improve the problem of Germanovix'a [6] method, Psychalinos[7], Yu [8]and Lopez-Martin[9-10] also adopted MOSFETs operating in saturation region to implement the square-root domain filters.

In this paper, a square-root domain filter with voltage supply down to 0.9V has been proposed. The paper is organized as follows: In Section 2, the principle and architecture of the square-root domain filter using state-space approach are derived and explained. Then in Section 3, the most supply-voltage critical block, i.e. the square-root circuit, which performs the geometric-mean function, is proposed to operate at a supply as low as 0.9V. By using the proposed circuit implementation as well as the state-space approach, several filter prototypes are designed for the purpose of verification highlighted in Section 4. Finally, a brief conclusion is given at the end of this paper.

2. Principle and Architecture

The transfer function of a second-order band-pass filter can be expressed as

$$H(s) = \frac{(\omega_0)s}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2} \quad (1)$$

By using the standard technique for deriving companion-form dynamical equations, Eq. (1) is realized with the system described by the following equations.

$$\begin{cases} \dot{x}_1 = -\omega_0 x_2 \\ \dot{x}_2 = \omega_0 x_1 - \left(\frac{\omega_0}{Q}\right)x_2 + \left(\frac{\omega_0}{Q}\right)u \\ y = x_2 \end{cases} \quad (2)$$

where x_1, x_2, y, and u are state variables, output and input signals, respectively. If the node voltages V_1 and V_2 are assumed to be the state variables, x_1 and x_2, and a voltage signal U denotes the input u, the Eq.(2) can be rewritten as

$$\begin{cases} C\dot{V}_1 = -C\omega_0 V_2 \\ C\dot{V}_2 = C\omega_0 V_1 - \left(\frac{C\omega_0}{Q}\right)V_2 + \left(\frac{C\omega_0}{Q}\right)U \\ y = V_2 \end{cases} \quad (3)$$

where C is a multiplicatioin factor. $C\dot{V}_1$ and $C\dot{V}_2$ in Eq.(3) can be regarded as the time-dependent current through the two capacitors C connected from V_1 to ground and from V_2 to ground, respectively.

The drain current of a MOSFET transistor operating in saturation can be expressed as

$$I_D = \frac{\mu_0 C_{ox} W}{2L}(V_{GS} - V_{th})^2 = \beta(V_{GS} - V_{th})^2 \quad (4)$$

where β, V_{GS} and V_{th} are the device trans-conductance parameter, the gate-to-source voltage and the threshold

voltage, respectively. Thus, the state-space equation becomes

$$\begin{cases} C\dot{V}_1 = -\sqrt{I_0 I_2} - I_T \\ C\dot{V}_2 = \sqrt{I_0 I_1} - \sqrt{\frac{I_0 I_2}{Q}} + \sqrt{\frac{I_0 I_U}{Q}} + I_T \\ y = V_2 \end{cases} \quad (5)$$

According to Eq. (4), and while supposing Q=1, the state equations in Eq. (3) can be written as

$$\begin{cases} C\dot{V}_1 = -\sqrt{I_0 I_2} - I_T \\ C\dot{V}_2 = \sqrt{I_0 I_1} - \sqrt{I_0 I_2} + \sqrt{I_0 I_U} + I_T \\ y = V_2 \end{cases} \quad (6)$$

where

$$\begin{cases} I_1 = \beta (V_1 - V_T)^2 \\ I_2 = \beta (V_2 - V_T)^2 \\ I_U = \beta (U - V_T)^2 \end{cases} \quad (7)$$

and

$$\omega_0 = \frac{\sqrt{\beta I_0}}{C} \quad (8)$$

$$I_0 = \frac{C^2 \omega_0^2}{\beta} \quad (9)$$

Note that ω_0 is inversely proportional to the capacitance C and is proportional to the square root of I_0; hence the cutoff frequency ω_0 is dominated by the capacitance C and I_0 is used to tune the cutoff frequency.

3. Circuit Implementation

3.1 Flipped-Voltage Follower Circuit

Fig. 1[3-5] shows a flipped voltage follower (*FVF*), which consists of a current source and two transistors. One transistor is cascaded with another. The current source supplies the drain current of M_1, and the voltage at the drain of M_1 connecting to the gate of M_2 can be expressed as

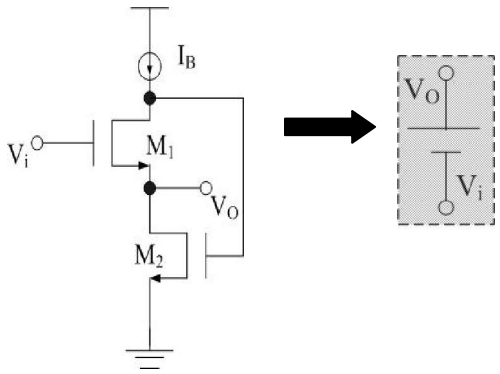

Fig.1. Current-mode Flipped-Voltage Follower (*FVF*) circuit

$$\begin{cases} V_{iO} \equiv V_{GS1} + V_{th} \\ V_{GS1} = \sqrt{\frac{I_B}{\beta}} \end{cases} \quad (10)$$

3.2 Current-Mode Square-Root Circuit

The proposed current-mode square-root circuit is shown in Fig. 2 operates as follows: I_X and I_Y are input currents, and these currents generate the corresponding voltage, V_X and V_Y through the current to voltage conversion of diode-connected MOS. The matched transistors M_2-M_5 which are forced to operate in saturation region and the DC current sources, depicted as I_C altogether to construct a voltage-averaging circuit.

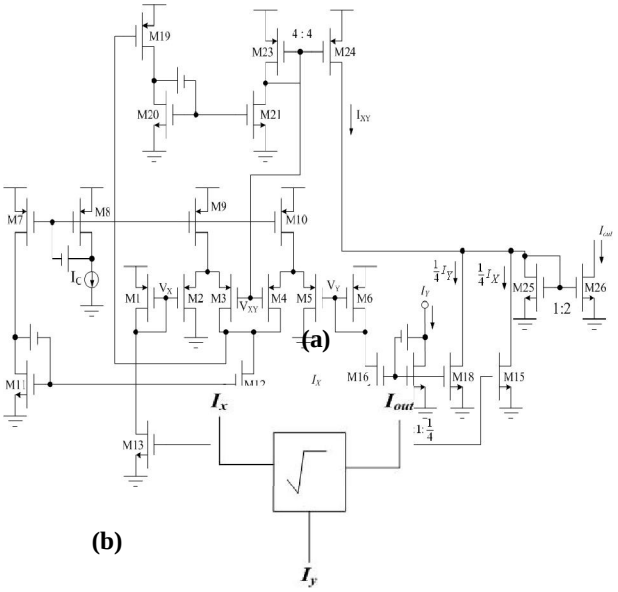

Fig. 2. Current-mode square-root circuit (a) Circuit diagram(b) Equivalent block diagram

The voltage averaging circuit produces a gate voltage V_{XY}, which is manipulated to be equal to the average of the gate voltage of M_1 and M_6 as V_{XY}= (V_X+V_Y)/2. The detailed operation of the averaging function circuit can be explained with a few simple steps. The well-known I-V relationship between the drain current and gate-source voltage for a MOS operating in saturation region can be formulated as the following equation:

$$I_D = \beta (V_{GS} - V_{th})^2 \quad (11)$$

We can easily find the following equation holds since I_{D2}+I_{D3}=I_{D4}+I_{D5}= I_C

$$I_{D2} = I_{D4} \quad (12)$$

Substitute Eq.(11) into Eq.(12) , the equation can be rewritten as

$$\beta (V_{S1} - V_X - V_{th})^2 = \beta (V_{S3} - V_{XY} - V_{th})^2 \quad (13)$$

From Eq.(13) we can derive the result :

$$V_{XY} = V_{S3} - V_{S1} + V_X \quad (14)$$

with the similar manner, we can obtain the following result.

$$V_{XY} = V_{S1} - V_{S3} + V_Y \quad (15)$$

According to Eq.(14) and Eq.(15), we can state the following Eq.(16).

$$V_{XY} = \frac{V_X + V_Y}{2} \quad (16)$$

According to the translinear loop formed by transistors M_X, M_Y, and M_{XY}, it is realized under the assumption of $\beta_{M23}=\beta_{M24} = 4\beta$ and $\beta_{M1} = \beta_{M6} = \beta$ where β is the aspect ratio, and the following equation can be derived.

$$I_{XY} = I_X + I_Y + 2\sqrt{I_X I_Y} \quad (17)$$

We narrow current I_X and I_Y by 1/4 times to give supply voltage of low power, so we can prove the following Eq.(17).

$$I_{XY} = \frac{1}{4}I_X + \frac{1}{4}I_Y + \frac{1}{2}\sqrt{I_X I_Y} \quad (18)$$

Again by writing the KCL equation at output node of this circuit, the equation can be reduced to the follows:

$$I_{XY} = \frac{1}{2}\sqrt{I_X I_Y} \quad (19)$$

Hence if the ratio of the output stage current mirror in Fig. 2 is set to be 1:2 the output current I_{out} can be derived as:

$$I_{out} = \sqrt{I_X I_Y} \quad (20)$$

Fig. 3 shows a circuit diagram of the proposed band-pass filter. The band-pass is realized by using current mirrors, three current-mode square-root circuit blocks and two capacitors. V_2 is the desired output voltage and U is a DC biased input voltage.

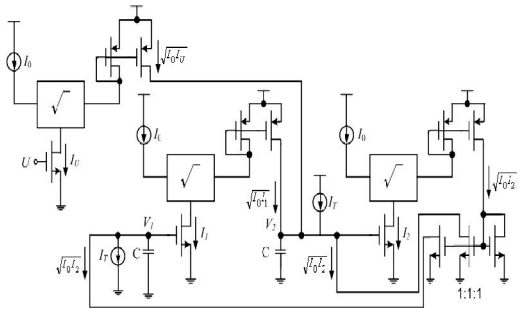

Fig. 3. Circuit diagram of the second-order band-pass filter

4. Simulation Results

Fig. 4 illustrates the simulated result of the current-mode square-root circuit while V_{DD} = 0.9V, I_X and I_Y are a triangular wave current with values between 20 to 30 μA and a 30 μA DC current, respectively.

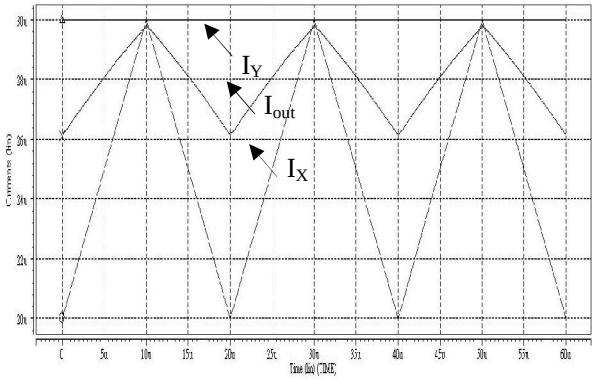

Fig. 4. Simulated result of the square-root circuit

The simulated frequency responses of the second-order band-pass filter with V_{DD} = 0.9V, C = 5 pf, Q = 1, I_0 is changed from 20 to 30 μA, shows the tunble center frequency f_0 of the band-pass filter from 776 to 914 kHz shown in Fig. 5.

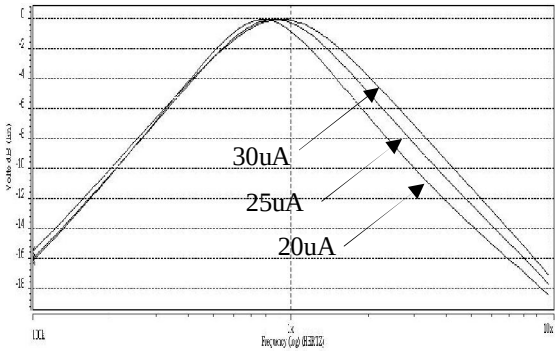

Fig. 5. Frequency response of the second-order band-pass filter

The total harmonic distortion (*THD*) with a 4MHz 100mV peak-to-peak sinusoid is 1.78%. The specifications of a second-order band-pass filter are summarized in Table 1.

Table 1. Specifications of the second-order band-pass filter

Parameters	**Simulation conditions**
Order of filter	2
Technology	TSMC 0.18μm
Power supply voltage	0.9V
Load capacitance	5 pf
I_0	20μa, 25μa, 30μa
Parameters	**Simulation results**
f_0 (I_0=20μa, 25μa, 30μa)	776kHz, 871kHz, 914kHz
Power dissipation (I_0=20μa, 25μa, 30μa)	387μW, 452μW, 487μW
THD (V_{PP}=0.1V) (I_0=20μa, 25μa, 30μa)	1.78%, 1.61%, 1.25%

5. Conclusion

In this paper, based on the MOSFET square law, a square-root domain band-pass filter with low voltage and low power operation is proposed. Operating at 0.9V power supply voltage, band-pass filter has been simulation in 0.18μm CMOS technology.

The proposed circuit, thus, has the advantages of high frequency operation, low supply voltage operation and low power consumption. Furthermore, implementation via standard digital CMOS technology for the proposed filter is feasible for system-on-a-chip (SOC) application.

References

1. RW Adams. Filtering in the log-domain. *AES Conj*, 1979, preprint 1470.
2. MH Eskiyerli, AJ Payne, C Toumazou. State-space synthesis of biquads based on the MOSFET square law. IEEE Int. Symp. Circuits and Syst, 1996;1:321–324.
3. Ramirez-Angulo I, Carvajal RG, Torralba A, *et al.* The flipped voltage follower: a useful cell for low-voltage low-power circuit design. lSCAS ,2002, Phoenix, AZ, pp. 111 615.618,
4. CA De La Cruz-Blas, AJ Lopex-Martin, A Carlosena. 1.5V tunable square-root Domain filter. *Electron. Lett*, 2004;40.
5. J Ramirez-Angulo, S Gupta, RG. Carvajal, *et al.* New improved CMOS class AB buffers based on differential flipped voltage followers. *IEEE Int. Symp*. Circuits Syst., Kos, Greece, May 21–24, 2006; 3914-3917.
6. W Germanovix, G. O'Neill, C Toumazou, *et al.* Analogue micropowered log-domain tone controller for auditory prostheses. *Electron. Lett*, 1998; 34: 1051-1052.
7. C Psychalinos, S Blassis. A systematic design procedure for square-root-domain circuits based on the signal flow graph approach. *IEEE Trans. Circuits Syst. I*, 2002;49:1702-1712.
8. G. J Yu, BD Liu, YC Hsu, *et al*. Design of log domain low-pass filters by MOSFET square law. *In Proc. The Second IEEE Asia Pacific Conf. on ASICs*, 2000, pp. 9–12.
9. AJ Lopez-Martin, A Carlosena. A 1.5 V CMOS companding filter. *Electron Lett*, 2002; 38: 1346–1347.
10. AJ Lopez-Martin, A Carlosena. A 3.3V tunable current-mode square-root domain biquad. *In Proc. IEEE Int. Symp. Circuits and Syst*.,2000; 5:375–378.