A review of the evolution of current-mode circuits and techniques and various modern analog circuit building blocks

Kasim K. Abdalla[1], D. R. Bhaskar[1], Raj Senani[2]

[1] Department of Electronics and Communication Engineering, Faculty of Engineering and Technology, Jamia Millia Islamia, New Delhi-110025, India
[2] Division of Electronics and Communication Engineering, Netaji Subhas Institute of Technology, Azad Hind Fauj Marg, Sector-3, Dwarka, New Delhi- 110078, India. Email: senani@nsit.ac.in

Abstract: This paper presents a brief introduction and review of some prominent current mode building blocks, which have been finding prominent attention in the area of analog signal processing. Some exemplary hardware implementations of a selected number of building blocks such as op-amp, OTA, CCI, CCII, FTFN, DDA, CFOA, CCIII, DDCC, DOCC, MOCC, DVCC, ICCII, FDCCII, OTRA, CDBA and CDTA have been reviewed.
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1. Introduction:

The development of very large scale integration (VLSI) technology, together with the ever increasing demand for fully integrated systems containing a larger number of digital as well as analog circuits on a single chip, has ensured continued interest on analog circuit design which is required to be compatible with CMOS technology. In fact, analog circuits such as continuous-time filters, sinusoidal oscillators, digital to analog (D/A) and analog to digital (A/D) converters, voltage comparators, current and voltage amplifiers, rectifiers, etc. are unavoidable analog circuits which can not be realized by digital techniques. Moreover, new applications continue to appear where new analog topologies have to be designed to ensure the trade-off between speed and power requirements.

Analog circuit design has historically been viewed as a voltage dominated form of signal processing. Recently, current-mode analog circuits have emerged in the implementation of analog functions. In current- mode circuit description, the input and the output are both taken in the current form rather than in voltage form. Current- mode signal processor can be defined as a circuit in which current is used as the active variable in preference to voltage, either throughout the whole circuit or only in certain critical areas.[19] In contrast to the conventional voltage mode circuits, the current mode circuits can exhibit, under certain conditions, among other things higher bandwidth and better signal linearity. Since they are designed for lower voltage swings, smaller supply voltages can be used.[95]

In addition to the advancement in current-mode analog signal processing, another particular development is the emergence of new current-mode analog building blocks among which the most prominent and popular has been the current conveyor (CC)[1, 3, 13]. The concept of the current conveyor was first introduced by Smith and Sedra in 1968. It was called the first-generation current conveyor (CCI)[1] which is a 3-terminal building block having three terminals X, Y, Z and the port variables characterized by $i_Y = i_X$, $v_X = v_Y$ and $i_Z = \pm i_X$. The second-generation current conveyor (CCII) was developed in 1970 [3] and is characterized by $i_Y = 0$, $v_X = v_Y$ and $i_Z = \pm i_X$ and further developed to the third-generation current conveyor in 1995 (CCIII) [23] which was characterized by $i_Y = -i_X$, $v_X = v_Y$ and $i_Z = \pm i_X$. Since then, the area of current mode circuits has progressed very fast and several thousand research papers have been published in this exciting area so far.

With different modifications in the basic conveyor structure, a number of newer elements have been introduced a brief account of which now follows. A second generation current controlled conveyor (CCCII) is characterized by $i_Y = 0$, $v_X = v_Y + i_X r_X$ and $i_Z = \pm i_X$ and was implemented in BJT technology by Fabre in 1995 [24] and in 1996 [26] and in BiCMOS technology in 1997. [28] Dual-output current conveyor (DO-CCII) [58] is characterized by $i_Y = 0$, $v_X = v_Y$, $i_Z^+ = i_X$, $i_Z^- = - i_X$, can provide two opposite direction outputs when the output terminals are in the same direction. Another variant is the so-called current follower current conveyor (CFCCII).[17] Inverting current conveyor (ICC) was introduced by Awad and Soliman in 1999 [33] is characterized by $i_Y = 0$, $v_X = - v_Y$ and $i_Z = \pm i_X$. Differential current conveyor (DCC) was presented by Elwan and Soliman in 1996 [25] which has two X terminals and the current of the Z terminal is given by the difference between the X terminals currents i.e., $i_Z = i_{X1} - i_{X2}$. Differential voltage current

conveyor (DVCC) was introduced by Elwan and Soliman in 1997 [29] which is a five terminal building block with two Y terminals such that $i_{Y1} = 0 = i_{Y2}$, $v_X = v_{Y1} - v_{Y2}$ and $i_Z = i_X$. A DVCC with two complementary current output terminals is known as DVCCC (Differential Voltage Complementary CC) [29] and provides $i_{Z1} = i_X$, $i_{Z2} = - i_X$. Differential difference Current Conveyor (DDCC) was presented by Chiu, Liu, Tsao, and Chen in 1996 [27], but when combining the effect of both DDCC+ and DDCC- in a single active building block (ABB) where two complementary current outputs are presented, it is known as differential difference complementary current conveyor (DDCCC) [48] and is characterized by $i_{Y1} = i_{Y2} = i_{Y3} = 0$, $v_X = v_{Y1} - v_{Y2} + v_{Y1}$, $i_{Z1} = i_X$, $i_{Z2} = - i_X$. Fully differential second generation Current Conveyor (FDCCII) was introduced by Alzaher, Elwan and Ismail in 2000 [37] where each of the terminals has been doubled with respect to the original CCII, but dual-X second generation current conveyor (DXCCII) introduced by Zeki and Toker in 2002 [50] has two X-terminals (X_p and X_n) as well as two related output Z terminals (Z_p and Z_n). Modified CCII (MCCII) was introduced by Dukic in 2007 [87] where the current through the output Z terminal (always positive) does not depend on the direction of X terminal current. An operational floating conveyor (OFC) was introduced by Toumazou and Payne in 1991.[16] Universal current conveyor (UCC) presented by Becvar, Vrba, Zeman and Musil in 2000 [40] is able to replace any type of existing current conveyor. Modified third generation current conveyor (MCCIII) has been presented by Kuntman, Cicekoglu and Ozoguz in 2002.[49] Current gain current conveyor (CGCCII) [58] is designed with an output terminal (Z) such that Z-terminal current is n times higher current with respect to X terminal current. Also there are a number of new variations of slightly different nature which incorporate such as current division network (CDN) [99] and digitally controlled current follower (DCCF) [88] in an appropriate manner to enhance the controllability of the relation between output and input currents.

The application of filters and oscillators in communication circuits needs extended high frequency performance in fully integrated circuit form. Circuit designers began to search for a more suitable active element in order to provide the unavoidable gain without imposing severe frequency limitations. At the same time, it was endeavored to keep the circuitry simple so that it can be realized in IC technologies enabling easy synthesis procedures for active circuits, hence, there are many active building blocks introduced for this purpose. The most widespread active element for on chip implementation is undoubtedly the operational transconductance amplifier (OTA) which was introduced by Wheatley and Wittlinger in 1969.[2] Bialko and Newcomb in 1971 [4] demonstrated how all basic linear functions can be realized using the integrated differential voltage-controlled-current-source (DVCCS). CMOS low-voltage OTA was introduced by Elwan, Gao, Sadkowski and Ismail in 2000.[39] The Multiple Output OTA (MO-OTA) has appeared as a generalization of Bipolar OTA (BOTA) and its applications were demonstrated in the design of economical biquadratic filters.[41, 61]

The need for the floating output in some applications led to the design of monolithic floating nullor.[6] The Four-terminal floating nullor (with the acronym 'FTFN' coined for the first time in [10-11] by Senani) has been shown to be a very flexible and versatile building block in active network synthesis. A number of papers have dealt with its implementation [6, 8, 11] and a general implementation has been described by Higashimura in 1991.[15] An FTFN is equivalent to an ideal nullor and it is also called operational floating amplifier (OFA). A technique for realizing a versatile OFA using an op-amp is presented by Nordholt in 1982.[7] An implementation of the operational floating amplifier (OFA) was introduced by Huijsing in 1990.[14] Differential difference amplifier (DDA) has four high-impedance inputs compared to conventional operational amplifier (Op-amp) which has two high impedance inputs, and it was introduced for the first time by Säckinger and Guggenbuhl in 1987.[9] Differential difference operational floating amplifier (DDOFA) is combining the advantages of the fully balanced input of DDA and the symmetrical output of OFA.[32] The concept of the fully balanced four-terminal floating nullor (FBFTFN) was introduced by Alzaher and Ismail in 2002 [52] who also gave its CMOS implementation and applications.

The conventional transimpedance operational amplifier (TOA) is a combination of the CCII and the voltage buffered amplifier.[12] Current feedback amplifier (CFA) [38] and TOA have an identical internal structure. The absence of electronic control of the voltage gain or any other parameter in the conventional Op-amp enforced designing the current-controlled CFA (CC-CFA).[89] Some interesting variants of CFAs have also been proposed such as differential voltage CFA (DVCFA) [53] and its further generalized form, namely, the differential difference complementary current feedback amplifier (DDCCFA) introduced by Gupta and Senani in [65] which was shown to be capable of realizing a number of prevalent building blocks.

A new active element termed as operational transresistance amplifier (OTRA) (commercially available as Norton amplifier [5, 44]) along with its CMOS implementation was introduced by Chen, Tsao

and Chen in 1992.[21] On the other hand, another new element known as current differencing buffered amplifier (CDBA) was introduced by Acar and Ozoguz in 1999.[34] There are numerous papers published employing CDBAs in various applications.[54-56, 62, 64, 68-69] CDBA is also known as differential current voltage conveyor (DCVC).[47] CDBA is basically a generalization of OTRA as an universal element. Current differencing unit (CDU) and the voltage unity-gain buffer are contained into the internal structure of the CDBA. CDU is a current conveyor of the MDCC type. A Current controlled CDBA (CC-CDBA) was presented by Maheshwari and Khan in 2004 [63], while a current differencing transconductance amplifier (CDTA) was introduced by Biolek in 2003 for the first time.[57] CDTA applications may not require the use of external resistors, which are substituted by internal transconductors, therefore many research papers were published employing CDTA.[66, 70-73, 75, 78, 80-84, 90-91] Current controlled CDTA (CCCDTA) was modified from CDTA by Siripruchyanun and Jaikla in.[85, 92, 96]

2. Hardware Implementation of Some Selected Analog building Blocks:

This section presents symbolic notation and hardware implementation circuits of some selected analog building blocks directly or indirectly related to the work presented in this thesis.

Operational amplifiers (op-amps) are one of the most widely used building blocks for analog circuits and systems. Op-amps are employed from dc applications to high speed amplifiers and filters. General purpose op-amps can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, and in many other applications. The op-amp is a differential voltage controlled voltage source. The symbolic notation of the op-amp is shown in Fig. 1.

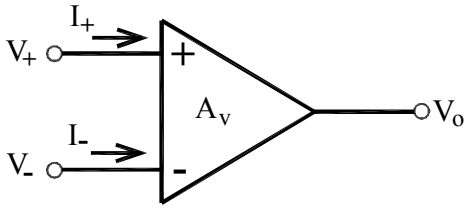

Fig. 1 Symbolic notation of the op-amp

The characterising equations of the op-amp are: $V_o = A_v(V_+ - V_-)$, where A_v = open-loop voltage gain.

A typical CMOS implementation of the op-amp is shown in Fig. 2.

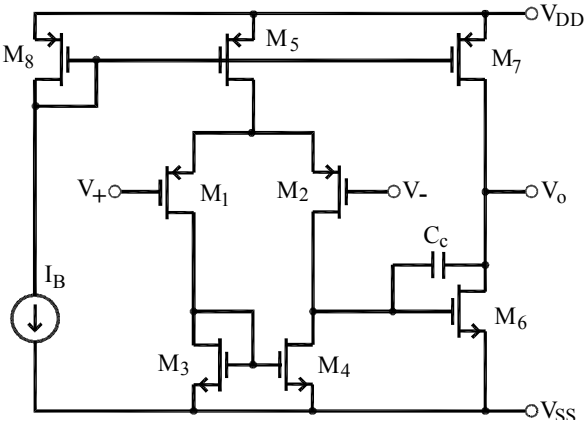

Fig. 2 CMOS realization of an op-amp adopted from.[8]

Operational transconductance amplifier (OTA) is a differential voltage controlled current source. Fig. 3 shows the symbol of OTA. For an ideal MO-OTA with transconductance g_m, the output current I_o is given by $I_o = \pm g_m (V_+ - V_-)$. The transconductance ($g_m$) can be varied by changing the bias current I_{bias}. The transconductance (g_m) of CMOS OTA is equal to $(\beta I_{bias}/4)^{1/2}$ (where $\beta = \mu C_{ox}(W/L)$) and of bipolar OTAs is $I_{bias}/2V_T$, respectively.[79]

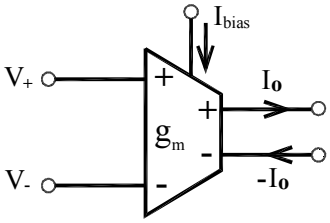

Fig. 3 Symbolic notation of OTA.

A representative CMOS realization of the MO-OTA is shown in Fig. 4.[35, 76]

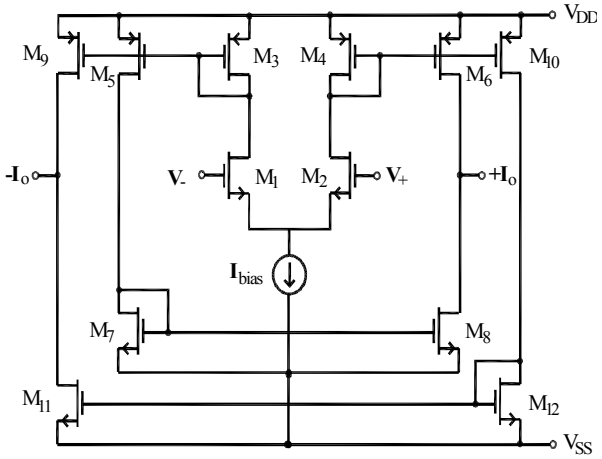

Fig. 4 CMOS realization of the MO-OTA proposed by Zeki and Kuntman.[35]

Out of a large number of elements proposed so far, current conveyors are the most popular active building blocks because of their superior and versatile terminal characteristics as well as their widespread applications which include amplifiers, oscillators, filters, wave shaping circuits, precision rectifiers and numerous others.

The first generation current conveyor CCI has been introduced in 1968 as the first CC. The CCI is a three terminal active building block with terminals labeled X, Y and Z as shown in Fig. 5.

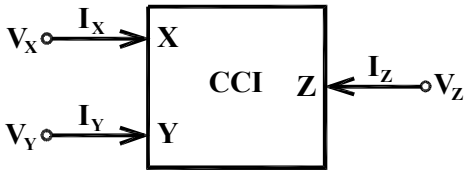

Fig. 5 Symbolic notation of CCI

The CCI± is characterized by the hybrid matrix:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \qquad (1)$$

where plus and minus signs denote a positive and negative CCI.

An exemplary CMOS implementation of CCI is shown in Fig. 6.

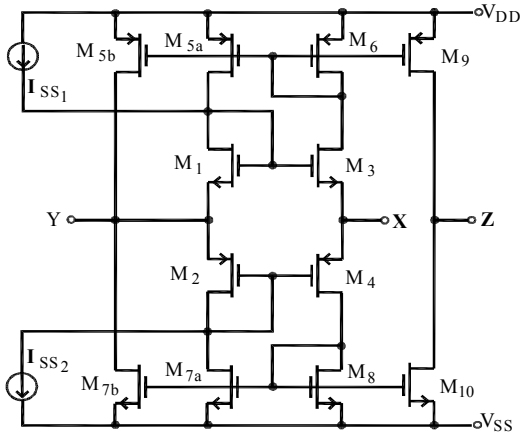

Fig. 6 An exemplary CMOS implementation of CCI proposed by Bruun.[22]

Second generation current conveyor CCII is the most versatile conveyor structure among all CCs and has shown to be useful in almost all analog circuit operations. The symbolic notation is shown in Fig. 7.

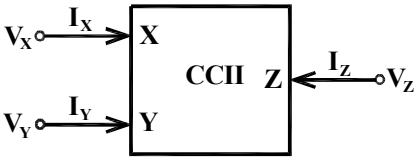

Fig. 7 Symbolic notation of CCII

For an ideal CCII, the relation between the voltages and currents is given by the hybrid matrix:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \qquad (2)$$

The CCII is defined in a positive and negative version, depending on the direction of the current in the Z terminal. Fig. 8 shows a typical CMOS implementation of the CCII+ [20].

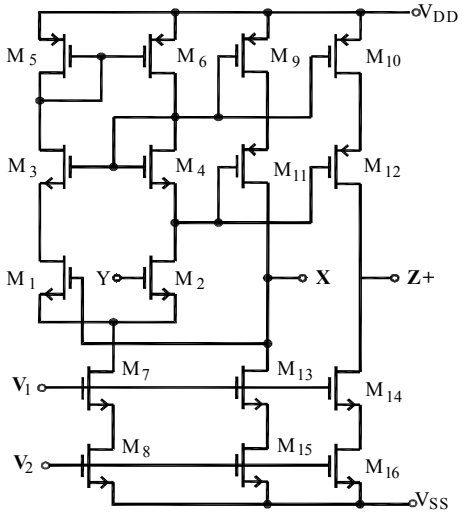

Fig. 8 A typical CMOS implementation of CCII+ proposed by Liu, Tsao and Wu[20]

That a four-terminal floating nullor (FTFN) is a very flexible and versatile building block in active network synthesis was demonstrated in.[10- 11, 18] The acronym FTFN has been introduced in 1987 by Senani for the first time in [10] and [11]. The symbolic notation of the FTFN is shown in Fig. 9.

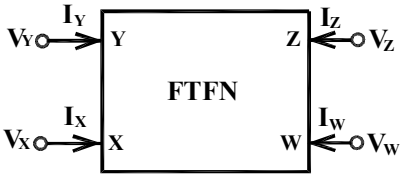

Fig. 9 Symbolic notation of FTFN

The port characteristics of an FTFN can be described as: $V_X = V_Y$, $I_X = I_Y = 0$, $I_Z = I_W$. Fig. 10 shows the CMOS realization of the FTFN.

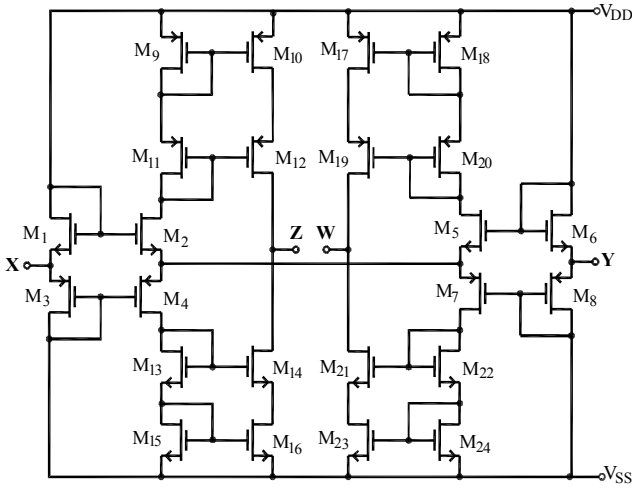

Fig. 10 CMOS realization of the FTFN proposed by Cam, Toker and Kuntman[43]

The Differential difference amplifier (DDA) is an extension to the concept of the op-amp. The main difference is that instead of two single-ended inputs as the case in op-amps, it has two differential input ports ($V_{pp} - V_{pn}$) and ($V_{np} - V_{nn}$) as shown in the Fig. 11. Therefore, the output of the DDA can be written as $V_o = A[(V_{pp} - V_{pn}) - (V_{np} - V_{nn})]$, where A is the gain of the DDA.

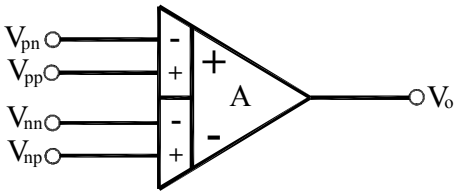

Fig. 11 Symbolic notation of the DDA

The CMOS implementation of the DDA is shown in Fig. 12.

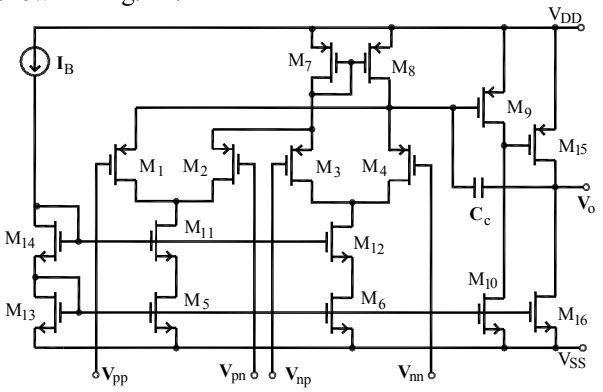

Fig. 12 CMOS realization of the DDA proposed by Säckinger and Guggenbuhl[9]

Trans-impedance operational amplifier or more popularly known as current feedback operational amplifier (CFOA) is receiving growing attention as an alternative building blocks for analog circuit design, because it offers several advantages over the traditional voltage–mode op-amp (VOA). Fig. 13 shows the symbolic notation of the CFOA.

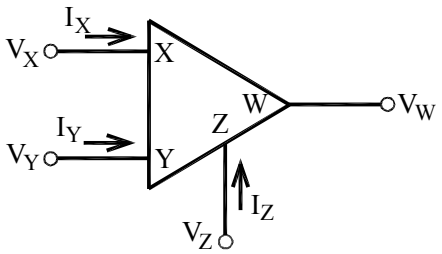

Fig. 13 Symbolic notation of the CFOA

The port relations of an ideal CFOA are described by the following hybrid matrix:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_W \end{bmatrix} \quad (3)$$

A CMOS implementation of the CFOA is shown in Fig. 14.

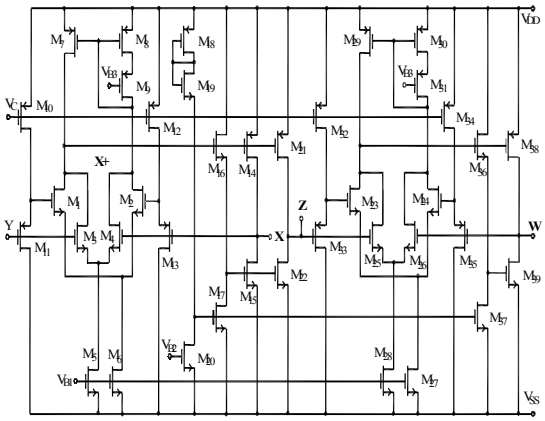

Fig. 14 A CMOS realization of the CFOA proposed by Mahmoud, Madian and Soliman[86]

Third generation current conveyors (CCIIIs) can be considered as current controlled current sources with a unity gain. This type of current conveyor is useful to take out the current flowing through a floating branch of a circuit and can be utilized in various multifunction filters, inductance simulation and active filters.[30, 31, 36, 45, 49] The terminal block diagram of an ideal dual-output CCIII is shown in Fig. 15.

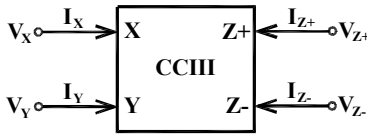

Fig. 15 Symbolic notation of CCIII

The defining hybrid matrix equation of a dual-output CCIII is given by:

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z\pm} \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (4)$$

A sample CMOS realization of the dual-output third generation current conveyor is shown in Fig. 16.

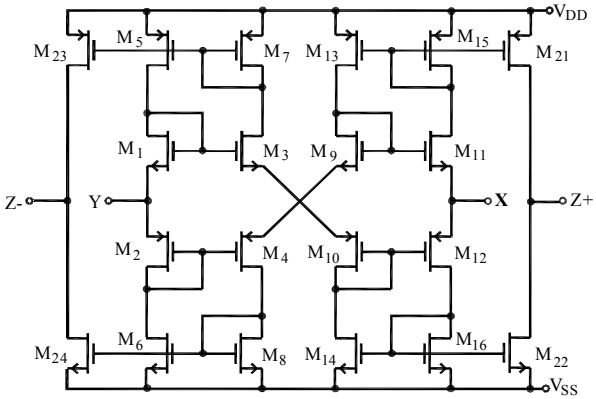

Fig. 16 A sample CMOS implementation of CCIII proposed by Minaei[59]

Differential difference current conveyor (DDCC) possesses the advantages of high input impedance at port Y_1, Y_2 and Y_3 and high output impedance at port Z which suits for voltage signal inputs and current signal output.[93, 97] Fig. 17 indicates the symbol of a DDCC.

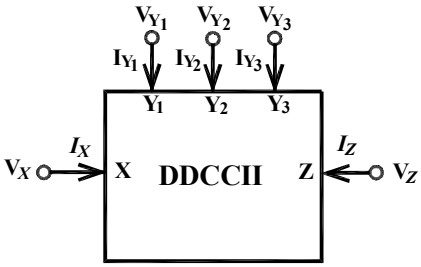

Fig. 17 Symbolic notation of DDCC

The port relations of an ideal DDCC can be characterized by:

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \pm 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_Z \end{bmatrix} \quad (5)$$

A typical CMOS implementation of the DDCC is shown in Fig. 18.

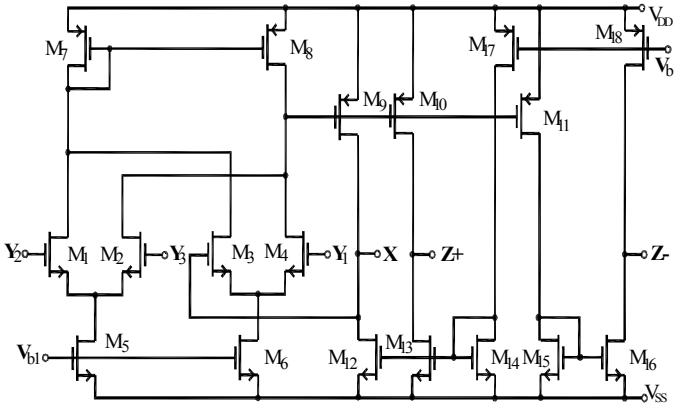

Fig. 18 A CMOS realization of the DDCC proposed by Hou and Lin [60]

Dual output current conveyor (DOCCII) is a four terminal building block. The two output terminals have opposite directions. The symbolic notation is shown in Fig. 19.

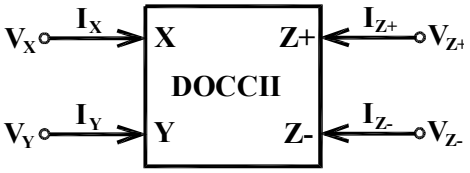

Fig. 19 Symbolic notation of DOCCII.

The ideal DOCCII can be characterized by:

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (6)$$

A sample CMOS DOCCII implementation of the DOCCII is shown in Fig. 20.

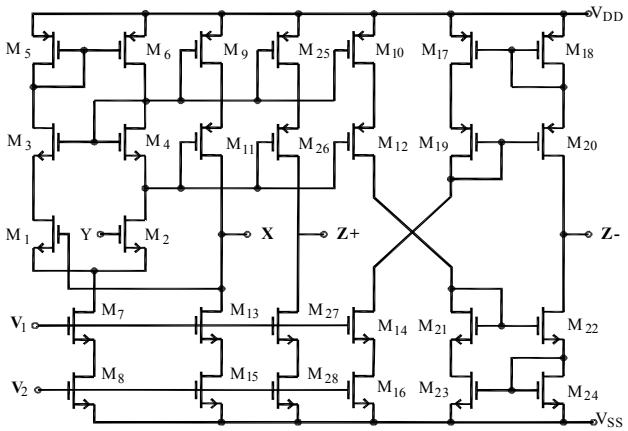

Fig. 20 CMOS realization of the DOCCII modified by Singh, V.K., Singh, A.K. and Senani [67] from the implementation of Liu, Tsao and Wu [20])

Multiple output current conveyor (MOCCII), which has multiple outputs, has its symbolic notation shown in Fig. 21.

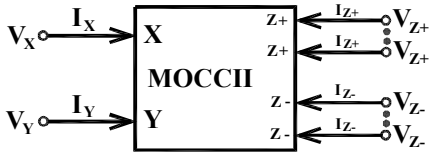

Fig. 21 Symbolic notation of MOCCII

The relation between the voltage terminals and current for an ideal MOCCII is given by the hybrid matrix:

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (7)$$

For CMOS implementation of MOCC, one can use DOCC by adding multiple number of positive or negative outputs.[51]

Differential voltage current conveyor DVCC is a four terminal device, which has two high input impedance at terminals Y_1 and Y_2 and low input impedance at terminal X.[74] The symbolic notation of the DVCC is shown in Fig. 22.

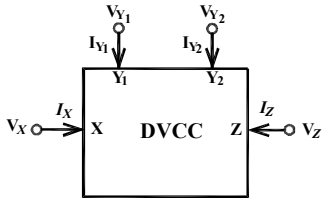

Fig. 22 Symbolic notation of DVCC

The ideal DVCC can be characterized by:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \end{bmatrix} \quad (8)$$

We can get the CMOS implementation of a DVCC, if we ground the terminal Y_3 of the CMOS DDCC [66], which is shown in Fig. 18.

The inverting second generation current conveyor (ICCII) is considered to be a special case from the DVCC or the DDCC. The symbolic representation of the balanced output ICCII is shown in Fig. 23.

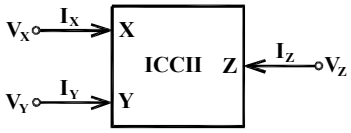

Fig. 23 Symbolic notation of ICCII

For an ideal ICCII the terminal characteristics in terms of current and voltage is given by the hybrid matrix:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (9)$$

For implementing ICCII+, the DDCC or the DVCC are employed [42, 46, 94], by grounding the terminals Y_1 and Y_3 of the circuit (DDCC) which is shown in Fig. 18.

Fully differential second generation current conveyor (FDCCII) is an eight-terminal analog building block shown symbolically in Fig. 24.

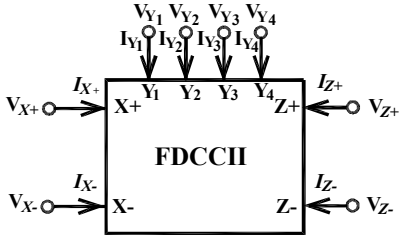

Fig. 24 Symbolic notation of FDCCII

The port relations of an ideal FDCCII are described by the following matrix equation:

$$\begin{bmatrix} V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & -1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X+} \\ I_{X-} \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \end{bmatrix} \quad (10)$$

A typical CMOS realization of the FDCCII is shown in Fig. 25.

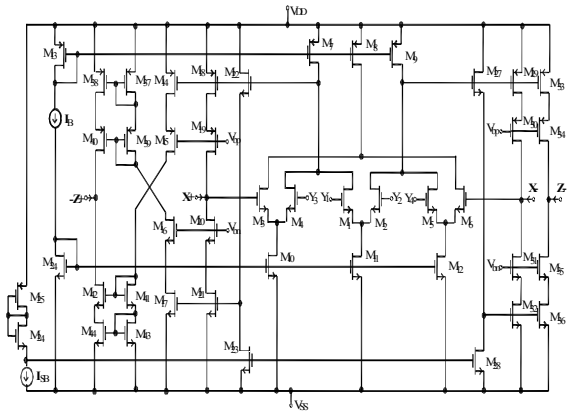

Fig. 25 CMOS realization of the FDCCII proposed by El-Adawy, Soliman and Elwan [77] and modified by Chen[98]

Some other types of active building blocks have also been frequently used in analog signal processing such as OTRA, CDBA, CDTA, etc.

Operational Transresistance Amplifier (OTRA) (commercially available, e.g. LM3900 and referred to as *Norton* amplifier) has attracted attention due to its advantages in the current-mode circuit design.[5] The symbolic notation is shown in Fig. 26.

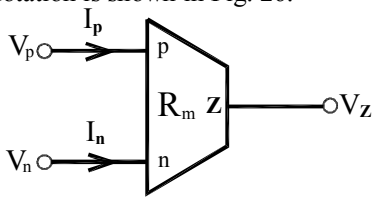

Fig. 26 Symbolic notation of OTRA

The ideal OTRA is characterized by:

$$\begin{bmatrix} V_p \\ V_n \\ V_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_z \end{bmatrix} \qquad (11)$$

A typical CMOS implementation of the OTRA is shown in Fig. 27.[21]

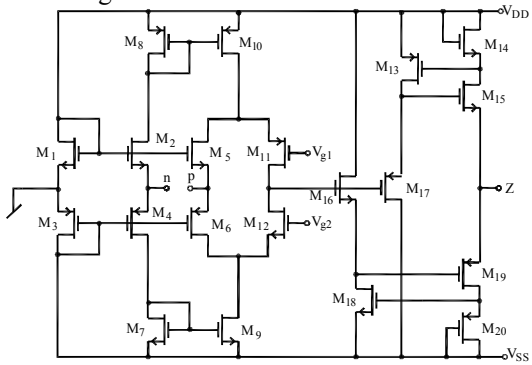

Fig. 27 CMOS realization of the OTRA proposed by Chen, J.J, Tsao and Chen, C.-C.[21]

The current differencing buffered amplifier (CDBA) has been found to be a versatile active building block for voltage- and current-mode signal processing applications. Fig. 28 shows the symbolic notation of the CDBA.

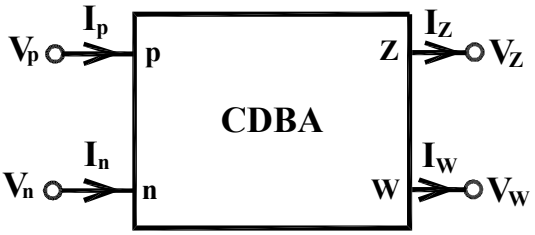

Fig. 28 Symbolic notation of the CDBA

The defining equations of the CDBA are: $V_p = V_n = 0$, $I_z = I_p - I_n$, and $V_W = V_Z$. A typical CMOS implementation of the CDBA is shown in Fig. 29.

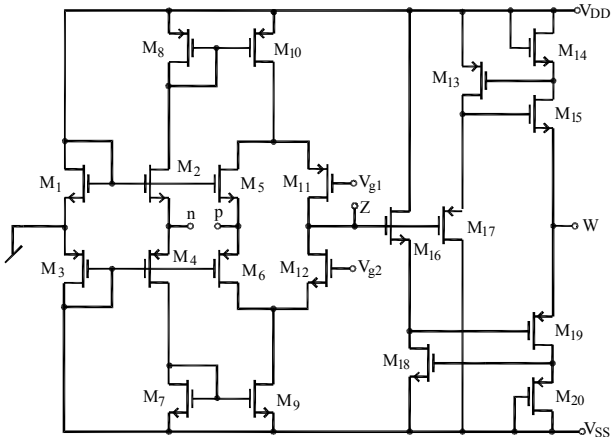

Fig. 29 CMOS realization of the CDBA proposed by Acar and Ozoguz[34]

Current Differencing Transconductance Amplifier (CDTA) is a five terminal active element and has recently been shown to be a versatile component in the realization of a class of analog signal processing circuits. It is actually a current-mode element whose input and output signals are currents. The symbolic notation of CDTA is shown in the Fig. 30. CDTA can contain an arbitrary number of X terminals, providing currents I_x of both directions. The port relations characterizing CDTA are given by $V_p = V_n = 0$, $I_z = I_p - I_n$, and $I_X = \pm g V_Z$, where g is the transconductance.

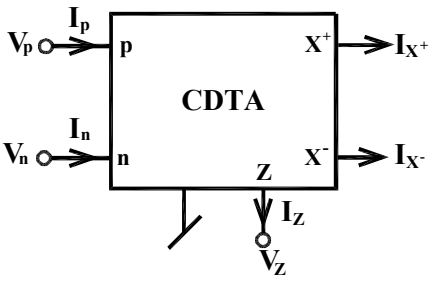

Fig. 30 Symbolic notation of CDTA

A representative CMOS implementation of the CDTA is shown in Fig. 31.

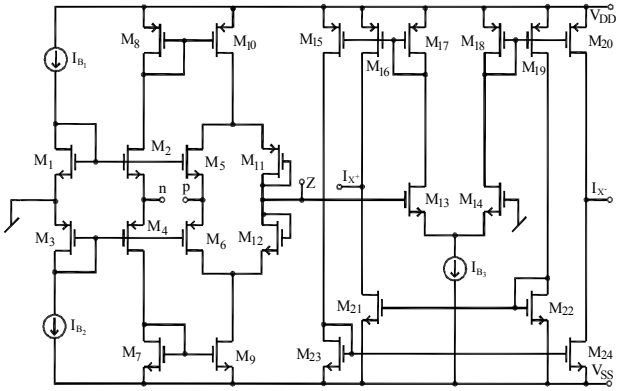

Fig. 31 CMOS realization of CDTA proposed by Keskin and Biolek[73]

A comprehensive treatment of a large variety of analog circuit building blocks, alongwith introduction of several new ones, has been dealt with in a recent paper by Biolek, Senani, Biolkova and Kolka.[95]

3. Concluding remarks:

This paper presented a brief introduction and review of some prominent current mode building blocks, which have currently been finding prominent attention in the area of analog signal processing. Some exemplary hardware implementations of a selected number of building blocks such as op-amp, OTA, CCI, CCII, FTFN, DDA, CFOA, CCIII, DDCC, DOCC, MOCC, DVCC, ICCII, FDCCII, OTRA, CDBA and CDTA have been reviewed. It is believed that this exposition would be useful to the analog circuit designers as well as beginners of research to acquaint them with some of the prominent building blocks and key ideas in the exciting area of analog circuit design.

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