Designing Of A new CMOS high ferquency Multiplier On Voltage Mode

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Abstract: A four-quadrant analog multiplier circuit, for low voltage supply and high frequency, is presented. Its advantages are as follow: it can be operating on low voltage supply, it can use either a single power supply or two power supplies, and all transistors used are the same dimension. The circuit is based on 90 nm CMOS technology simulated using HSPICE. The circuit operates using the supply voltage of ±1V and the cut off frequency is 4.57 GHz.

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Keyword: Multiplier; high frequency; low voltage

1. Introduction

Analogue four-quadrant multipliers find many applications in modern analogue VLSI signal and information processing. They are required for modulation/demodulation, detection, frequency translation, automatic gain controlling, Fuzzy systems and neural networks. Usually, the variable transconductance technique which operates on Gilbert's translinear circuit is widely used for the design of multiplier circuits in Bipolar and CMOS technologies [1]. The other approaches in CMOS technology are based on square-law characteristics of MOS transistor which are biased in saturation region [5] and that based on the current-voltage characteristics of MOS transistor in the nonsaturation region [4]. However, all mention techniques require resistors to obtain the output signal in voltage form. The use of resistors may require external resistors, which occupy large chip area to implement in IC form and also cause of the multiplier frequency degradation.

This paper proposes a multiplier that uses adder circuit with squaring circuits to get the quarter square algebraic identity.

2. Circuit Description

The principle of the proposed multiplier is based on the quarter-square algebraic identity:

$$(V_1+V_2)^2-(V_1-V_2)^2=4V_1V_2 \quad (1)$$

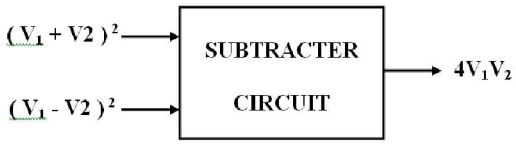

Fig 1: diagram of proposed circuit

In relation (1) V_1 and V_2 are input voltages. Therefore, the circuit needs summing, and squarer circuits. The summation and subtraction between two input voltages are firstly performed, then the results are squared. Finally, the multiplication is obtained by subtracting the square of the difference from the square of the sum.

2.1. Calculation of the squarer circuit

Considering the circuit in Fig 2, while both transistor work in saturation region.

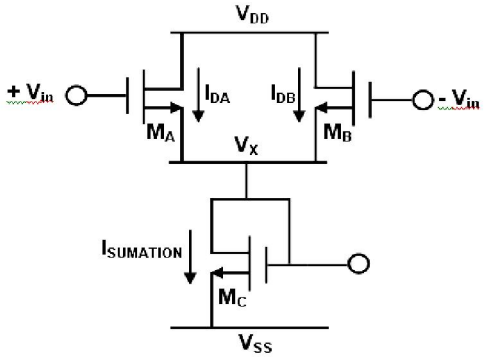

Fig 2: Squaring circuit

The currents through the transistors can be expressed as:

$$I_{DA}=0.5\,\mu_{n1}C_{OX1}W/L_1\left(V_{GS1}-V_{Tn1}\right)^2 \quad (2)$$

$$I_{DB}=0.5\,\mu_{n2}C_{OX2}W/L_2\left(V_{GS2}-V_{Tn2}\right)^2 \quad (3)$$

$$\text{奥}=\mu_nC_{OX}\left(W/L\right) \quad (4)$$

$$V_{GS}>V_{Tn}\ ,\ V_{DS}>=V_{GS}-V_{Tn} \quad (5)$$

Where K is the parameter of transistor, μ_n is the electron mobility, C_{OX} is the gate oxide capacitance per unit area, W/L is the transistor aspect ratio, V_{GS} is the gate- source voltage, V_{DS} is the drain-source voltage and V_{Tn} is threshold voltage of the MOS transistor. Suppose all transistors are identical, then $K_1=K_2=K$ and $V_{Tn1}=V_{Tn2}=V_{Tn}$ and:

$$I_{SUMATION} = I_{DA} + I_{DB} \tag{6}$$

$$I_{SUMATION} = K/2\left[\left(+V_{in}-V_X-V_{Tn}\right)^2+\left(-V_{in}-V_X-V_{Tn}\right)^2\right] \tag{7}$$

$$I_{SUMATION} = K\left[V_{in}^4+2V_{in}^2\left(V_{ss}+2V_{Tn}\right)^2+\left(V_{ss}+2V_{Tn}\right)^4\right] / 4\left(V_{ss}+2V_{Tn}\right)^2 \tag{8}$$

For small signal of V_{in}, it can be assumed that $V_{in}^4 \approx 0$. Then, the output current can be expressed as the simple input signal squarer as follows:

$$I_{SUMATION} = K/2V_{in}^2 + K/4\left(V_{ss}+2V_{Tn}\right)^2 \tag{9}$$

The voltage at V_X can be derived from using small signal model that is:

$$V_X = K/2g_mV_{in}^2 + K/4g_m\left(V_{ss}+2V_{Tn}\right)^2 \tag{10}$$

2.2. Subtraction and sumation circuit

The relationship of the drain current of transistors M_1-M_2 , M_3-M_4 is:

2.2.1. Subtraction circuit

$$I_{D1} = I_{D2} \tag{11}$$

$$I_{D3} = I_{D4} \tag{12}$$

$$K\left(V_1-V_{Out1}-V_{Tn}\right)^2 = K\left(V_2-V_{SS}-V_{Tn}\right)^2 \tag{13}$$

$$K\left(-V_1-V_{Out2}-V_{Tn}\right)^2 = K\left(-V_2-V_{SS}-V_{Tn}\right)^2 \tag{14}$$

The output voltage of signal subtraction circuit is:

$$V_{Out1} = V_1 - V_2 + V_{SS} \tag{15}$$

$$V_{Out2} = -V_1 + V_2 + V_{SS} \tag{16}$$

$$V_{OUT\,(SUB)} = V_{Out1} ? V_{Out2} = 2\left(V_1 ? V_2\right) \tag{17}$$

2. 2.2. sumation circuit

$$I_{D5} = I_{D6} \tag{18}$$

$$I_{D7} = I_{D8} \tag{19}$$

$$K\left(V_1-V_{Out3}-V_{Tn}\right)^2 = K\left(-V_2-V_{SS}-V_{Tn}\right)^2 \tag{20}$$

$$K\left(-V_1-V_{Out4}-V_{Tn}\right)^2 = K\left(V_2-V_{SS}-V_{Tn}\right)^2 \tag{21}$$

The output voltage of signal sumation circuit is**:**

$$V_{Out3} = V_1 + V_2 + V_{SS} \tag{22}$$

$$V_{Out4} = -V_1 - V_2 + V_{SS} \tag{23}$$

$$V_{OUT(SUM)} = V_{Out1} ? V_{Out2} = 2\left(V_1+V_2\right) \tag{24}$$

2.3 Calculation of the output voltage

The principle of the proposed multiplier is based on the quarter-square algebraic identity, that Is:

$$(V_1+V_2)^2 - \left(V_1 \text{ 朧 } _2\right)^2 = 4V_1V_2 \tag{25}$$

Employ the squaring circuit of Fig. 2 and the sumation-subtraction circuit of Fig 3.A and Fig 3.B, the analog multiplier can be realized as shown in Fig 3.

The sumation and subtraction outputs from these stages are applied to the squarer circuits formed by M_9, M_{10}, M_{13} for summing and M_{11}, M_{12}, M_{14} for difference, and the squarer outputs are through M_{13} and M_{14} [3]. The subtraction between squarer summing and squarer difference gives the result of multiplier in voltage mode.

$$V_{OUT} = K/2g_m\left(V_{OUT(SUM)}^2 - V_{OUT\,(SUB)}^2\right) \tag{26}$$

$$V_{OUT} = K/2g_m[(2\left(V_1+V_2\right))^2 - (2\left(V_1-V_2\right))^2] \tag{27}$$

$$V_{OUT} = \beta\, V_1V_2 \tag{28}$$

$$\beta = 8K/g_m \tag{29}$$

Results

The performance of the proposed analog multiplier circuit is simulated using PSPICE with level

54 model of 90 nm MOS parameter from MOSIS [2]. The complete circuit of the multiplier is shown in Fig 2 and the simulation uses 90 nm CMOS with L/W = 0.5/2 (μm), the supply voltage VDD = +1V and VSS = -1V. Since the drains of all squarer transistors (M_9, M_{10}, M_{11}, and M_{12}) are connected to V_{DD}, they must work on the saturation region. Set V_1 and V_2 between -100mV to and +100mV**.**

Fig 4 (A, B, C) shows the transient analysis of the multiplier as amplitude modulator. The modulation is performed when the input voltage V_1 and V_2 are respectively 30KHz and 1KHz sinusoidal input signals with peak amplitude of 100mV.

Fig 4 (D) shows the DC transfer characteristics of the proposed analog multiplier without any load. The output voltage swings between -11mV and +11mV for the input voltage range of ±100mv. Fig 4 (E) shows the frequency response.

Table 1 shows the performances of the multiplier. The multiplier has GHz-bandwidth response with low power consumption. The circuit has supply voltage ± 1 V. The proposed circuit has achieved -3dB bandwidth of 4.57 GHz.

Conclusion

A voltage-mode four-quadrant analog multiplier based on simple summation-subtraction and squaring circuits is proposed. The circuit is based on the simple square mathematics model that implements simple operational transconductance amplifier pairs and squaring circuit.

The circuit is based on the simple square mathematics model that implements simple operational transconductance amplifier pairs and squaring circuit. It achieves the multiplied output signal in voltage form without using resistors. The design uses 90 nm CMOS process and the performance has been demonstrated by using HSPICE. The circuit has the bandwidth 4.57GHz. This proposal than last model [3] have the senior frequency response and the very less using transistor that this is very important in the integration.

Table 1: performance of the multiplier

Number of MOS	14
Supply	±1V
W/L	0.5μ/2μ
Input range	± 100mV
Output range	± 11mV
-3dB freq response	4.57 GHz

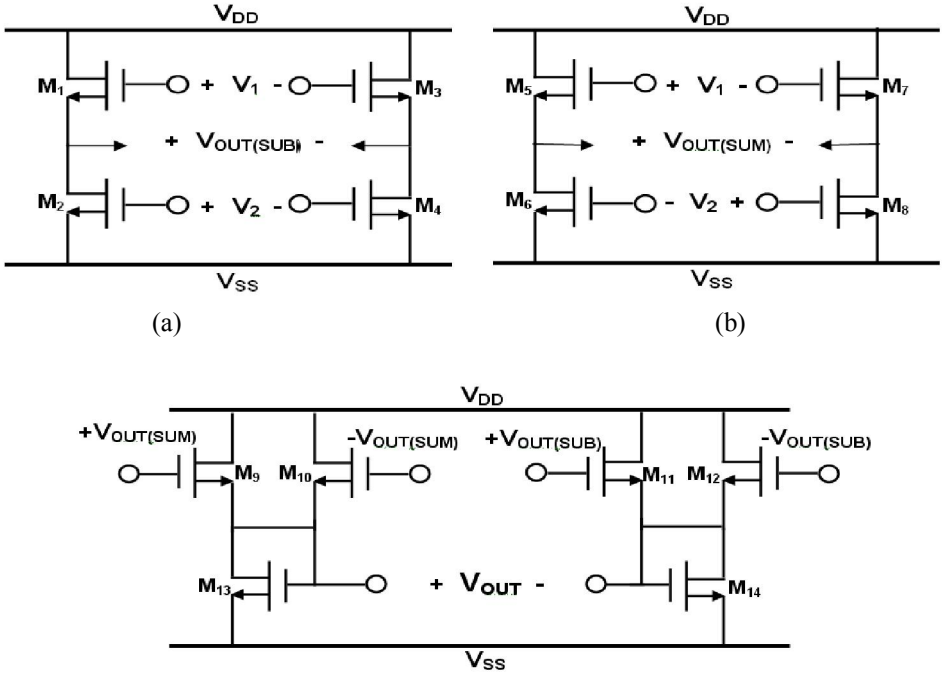

Fig 3: A. The summation circuit, B. The subtraction circuit, C. The proposal of analog multiplier circuit

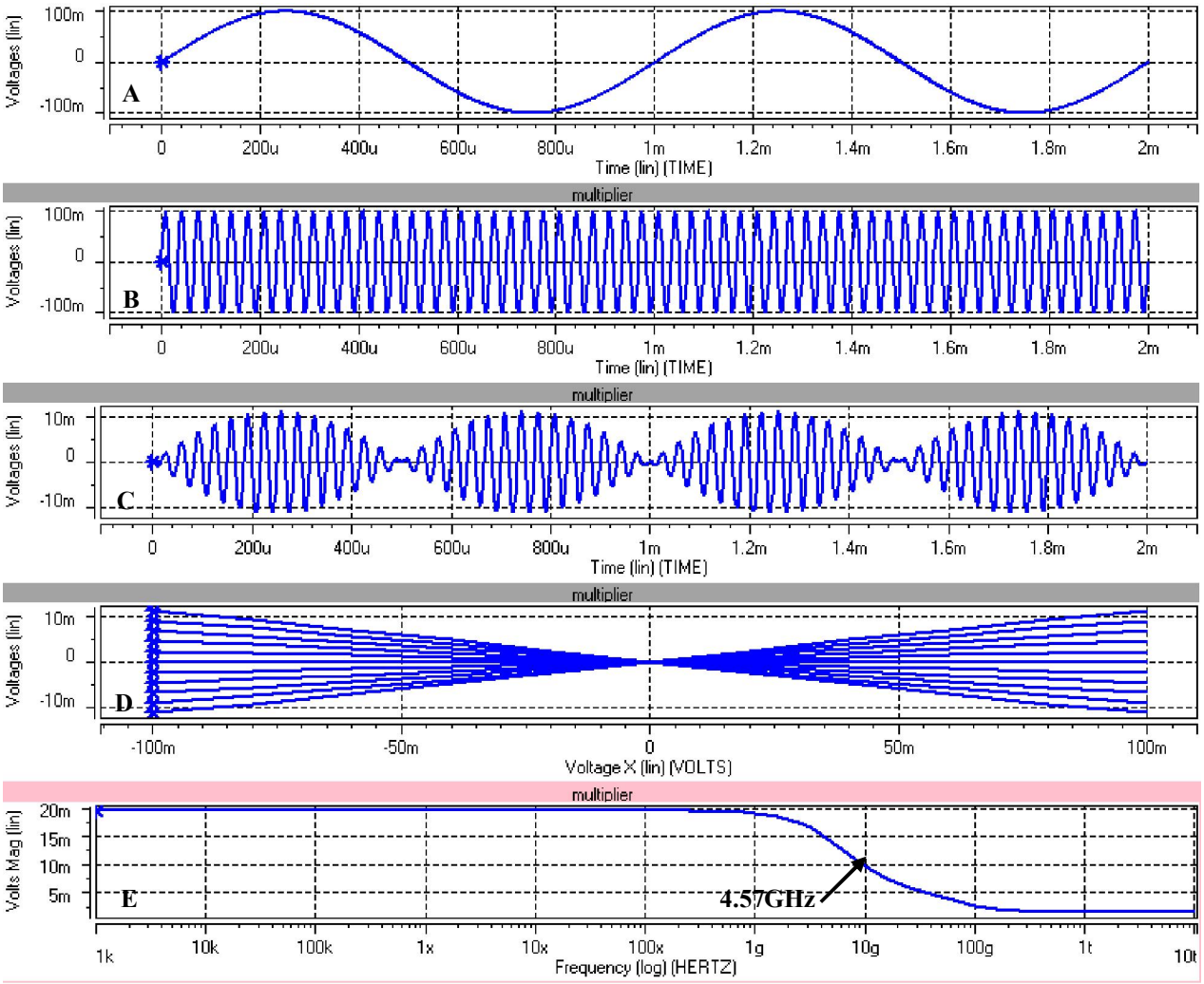

Fig 4: (A, B, C) The transient analysis of the multiplier as an amplitude modulator , (D) DC transfer characteristics (E) The frequency response

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